Silicon Models of Visual Cortical Processing

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ABSTRACT

Receptive field structures found in the visual cortex of the mammalian brain act as oriented, localized spatial frequency filters. There has been recent interest in the use of such receptive field profiles for image coding and texture processing. These receptive field structures resemble Gabor filters. Systems employing such Gabor filters have been implemented in software for a variety of applications. We believe a hardware implementation of such cells will be helpful in artificial visual processing. We have implemented analog VLSI cells whose outputs resemble the receptive field profiles found in the visual cortex. We describe experimental results of our circuit. Our circuit is the first silicon model of visual cortical processing.

I. Introduction

Neurons found in the primary visual cortex i.e. the striate cortex of the brain act as localized spatial frequency filters[11]. The receptive field profiles of such cells resemble even-symmetric or odd-symmetric Gabor filters. There are two classes of orientation-selective cells found in the visual cortex[5]. The cells have two principal subregions: one excitatory and the other inhibitory, and another class of cells with a central ON or OFF region flanked on both sides by an antagonistic surround. The profile of the first class of cells resembles a localized sine wave and the second class a localized cosine wave both possibly localized by a Gaussian-like profile. The first class of cells selectively respond to an edge and the second class responds to bar width. There are two schools of thought over the function of the visual cortical neurons. Some researchers believe that the visual cortical neurons act as feature detectors [12] while others believe that cortical neurons act as spatial filters [10, 8]. Each view has its own advantages and both views have very strong correlations. A nice argument in favor of feature detection is presented in [7]. In the next section we will describe the sine, cosine and Gabor analog VLSI circuits and show experimental results. In the third section we will describe possible applications of our cell. Finally we will summary our contribution.

II. Analog VLSI Implementations

We present our circuits as working models of visual cortical processing. The output of the circuits described below closely resemble the experimental receptive field profiles found in single cell recordings from the cat's visual cortex [6]. We have not, however, modeled the complex dendritic processing that precedes such cells and it is the focus of our future work. The input to our circuit is, therefore, assumed to be a linear voltage representation of space.

A. Sine Approximation Circuit

The circuit implementation of a temporal sine wave is well known and is now considered trivial. The same argument does not hold for a sine wave with respect to an independent variable such as an input voltage. There have been two earlier implementations, one using BJTs [13] and the other using MOS transistors [1]. Both the implementations are similar and use the differential current representation. The normalized output results in a sine wave like profile. Both circuits are designed using the translinear analysis technique. Most circuits, however, are single ended rather than differential representations. We have designed such a single ended implementation. Our circuit closely follows the implementation given in [1].

The output of the bump circuit presented in [3] is fed as the bias current to a differential amplifier. If the input to the differential amplifier is similar to the input of the current correlator then the currents in each limb of the differential amplifier will resemble one half of a Gaussian wave. This input is done by mirroring the current

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in the input limbs of the bump circuit to the limbs of the differential amplifier by means of an additional diode connected transistor. The circuit implements the following equation.

$$I_{out} = I_b \sec h^2\left(\frac{\kappa \Delta V}{2}\right)\tanh\left(\kappa^2 \Delta V\right) + I_{dc} \quad (1)$$

Where $\Delta V = V_1 - V_2$ and I_{dc} is the dc offset current

The complete circuit diagram is shown in Fig. 1. Transistors m1-m7 form a PMOS version of the bump circuit [3]. Vc determines the zero crossing of the sine circuit. Vbias is the bias voltage to the circuit. This bias must be sufficiently high in order to supply sufficient current to the diode connected transistors m6-m9. This is necessary to generate sufficient voltage levels to the tanh circuit [9] formed by transistors m10-m13 because the sources of the differential pair transistors m10-m11 are not at ground potential. The output of the circuit is shown in Fig. 2. The effect of different biasing levels is shown. If the biasing level is slowly increased the bump output becomes wider, quadratic and then finally flat. For proper circuit operation the bias voltage needs to be at least a few hundred millivolts above threshold. Transistors m15-m16 set a dc offset to the circuit so that the output of the circuit is able to vary in the positive and negative direction. In the mammalian retina there is a dc component in any visual representation, the dc level being the mean luminance of the pattern[4]. The input to these transistors are held at Vdd/2 for proper operation. Transistor m14 converts the voltage representation into a current representation.

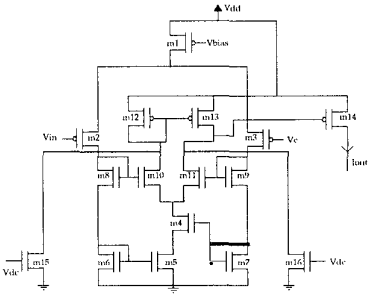

Figure 1. The Sine circuit

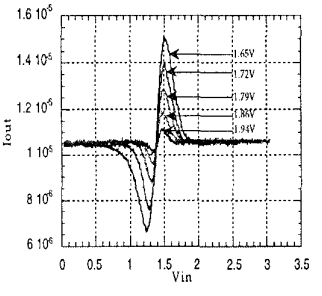

Figure 2. The measured output currents for different bias voltages to the Sine approximation circuit. Vc was held at 1.4 volts.

B. Sine Logon circuit

The sine logon is obtained by modulating a sine grating by a bivariate Gaussian. We, however, generate the sine logon profile by modulating the output of an edge detection unit by a Gaussian whose input is orthogonal to the input of the edge detection unit. Both profiles resemble each other. The bias of the sine circuit shown in Fig. 1 is replaced by the circuit presented in [14], and is shown in Fig. 3.

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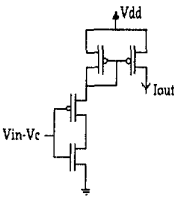

Figure 3. Our Gaussian cell

The sine logon circuit is shown in Fig. 4. In the Gaussian circuit, the PMOS and NMOS transistors in series act as complementary current correlators. The drain connected PMOS load serves to keep the circuit in the subthreshold region of operation for a large part of the input and also facilitates the mirroring of the current. For symmetrical operation Vdd is kept at 3V. A more detailed description is given in [14]. An advantage of using this circuit is it supplies higher currents. The need for a higher current occurs because the diode connected transistors m7 and m8 need sufficient input current to generate voltage ranges which allow the differential amplifier to operate properly. Another advantage is that this circuit can be easily made multidimensional as shown in [14]. This allows the input to be complex features such as lines. We however show results only from the simple implementation. The bias current effectively controls the amplitude of the sine wave and when modulated by a bias current results in a sine logon-like profile. The results from this circuit are shown in Fig. 5. The dc level in the circuit can be varied by changing the gate voltage on m15-m16 giving rise to very interesting properties which have biological counterparts. If the dc level is smaller than Vdd/2 then the negative lobe of the sine logon is smaller than the positive lobe. If the dc level is bigger the negative lobe dominates. There are receptive fields found in the visual cortex of the cat which have such profiles[6]. The same argument holds for the cosine logon circuit presented below.

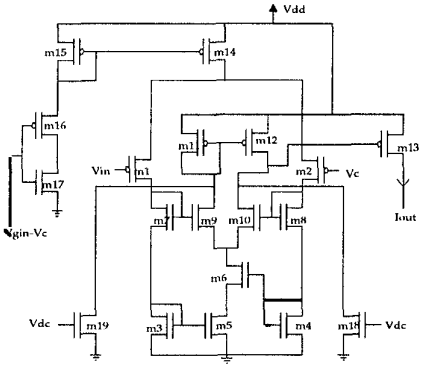

Figure 4. The Sine Logon approximation circuit.

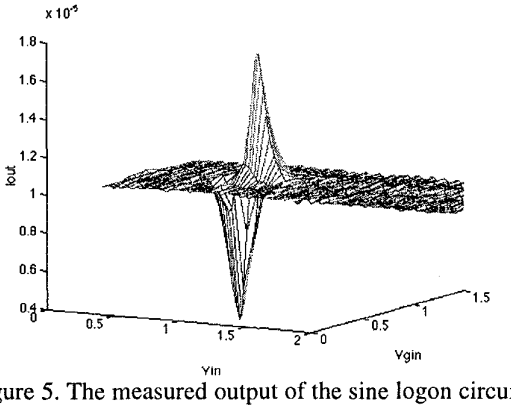

Figure 5. The measured output of the sine logon circuit

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C. Cosine approximation circuit

This circuit implements an on center off surround profile which resembles a localized cosine wave. A circuit for generating a cosine wave using BJTs is given in [13]. We, however, use our own implementation using MOS transistors. Our implementation uses lesser number of transistors.

The circuit is shown in Fig. 6. Transistors m1-m7 implement the bump circuit [3]. The output of the bump circuit is fed as a bias current to the differential amplifier. Also the bump circuit output is fed as an input to the differential amplifier. If the other input to the differential amplifier is a voltage that lies near the tail of the bump circuit then a cosine-like output results. Since we do not know this voltage *a priori* simple biases will not suffice. We will now consider the design of such a bias. Intuitively we know that the peak current occurs when the input to the differential amplifier are equal. Thus, if we duplicate this circuit and keep the inputs equal to the center voltage we can obtain a current that is equal to the current at the peak. But we need the current to be slightly smaller, therefore we have to make the ratio of the correlating transistors of the bias circuit slightly smaller than the ratio used for the bump circuit. We used ratios of .5 for the bump circuit and .48 for the bias circuit. This ratio is calculated assuming equal currents in both limbs to simplify the calculation. This elaborate bias is done to provide robustness to fabrication variations. Transistors m8-m14 forms the bias circuit, and m15, m16, m20 and m21 are the diode connected mirroring transistors. Transistors m17-m19 and m22-m23 form the differential amplifier, and m24 converts the voltage to current representation. Transistors m25-m26 forms the dc current bias to the circuit. The experimental output of the circuit is shown in Fig. 7.

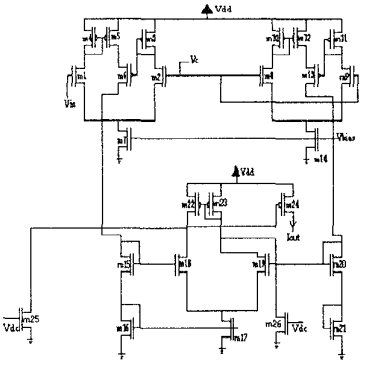

Figure 6. The Cosine approximation circuit

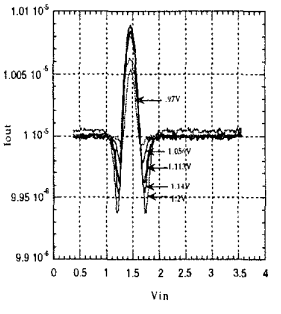

Figure 7. The measured output of the cosine circuit. The longer negative tails for higher bias voltages are due to the increased dominance of the negative input of the output differential amplifier.

D. Cosine Logon circuit

The cosine logon is designed using the same design philosophy as the sine logon circuit. The complete circuit is shown in Fig. 8. The experimental output of the circuit is shown in Fig. 9.

An important property of both the sine and cosine approximation is that we can get both in phase and 180^{o} out of phase in case of the sine and OFF or ON center in case of the cosine depending on whether we compute I_1-I_2 or I_2-I_1, the currents representing the limb currents in the differential amplifier.

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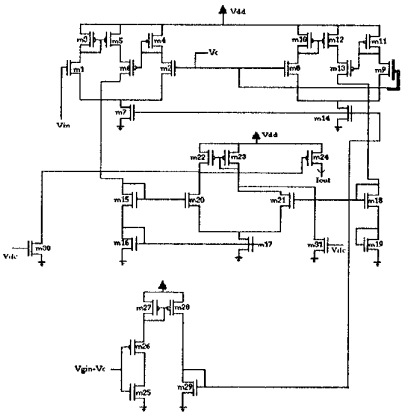

Figure 8. The Cosine Logon approximation circuit.

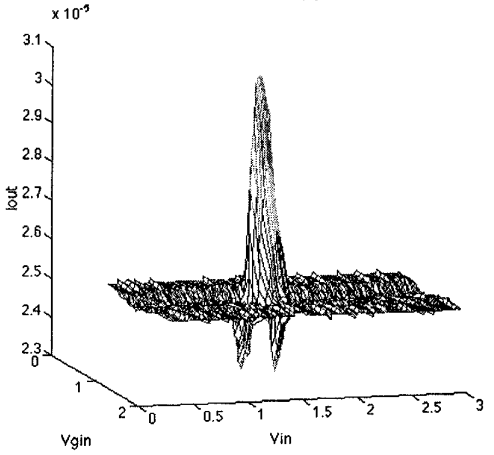

Figure 9. The measured output of the cosine logon circuit

III. Applications

Some of the possible applications of our circuits are listed below. There is evidence that the spatial information in rats may be encoded by phasors i.e. the phase and amplitude of a sine wave[15]. Our sine approximation circuit can be used in this case. The amplitude can be controlled by the bias and the phase by the center. The sine and cosine cells can be used as feature detectors in a neural network used for image coding. The Gabor circuit can be used in image compression networks like the one presented in [2]. All the applications do, however, require an efficient space domain to voltage domain transfer.

IV. Conclusion

Visual cortical neurons behave both as localized spatial frequency filters and simple feature detectors. We have presented compact analog VLSI circuits which have similar receptive field profiles as visual cortical neurons. We believe that such cells will be very useful in artificial visual processing. The cells presented may be used as Gabor filters or as simple cells. Simple cells being edge and On-Off center cells.

V. References

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