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Micro Power Delta-Sigma Analog-to-Digital Converters based on Novel Self-Biased Inverter Amplifiers

A Dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

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December 2010

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ABSTRACT

Micro Power Delta-Sigma Analog-to-Digital Converters based on Novel Self-Biased Inverter Amplifiers

by

Le Wang

This dissertation work presents the design and implementation of micro power switched-capacitor delta-sigma analog-to-digital converters for neural recording systems. Novel self-biased fully differential inverter amplifiers are proposed to replace conventional operational amplifiers for achieving high power and area efficiency. By responding to differential-mode and common-mode signals in different ways, the proposed inverter amplifiers show high differential-mode gain and common-mode rejection, which are advantageous compared to a pseudo-differential input pair. The operation principles and analytical models of the inverter amplifiers will be discussed in the dissertation. To realize inverter amplifier-based switched-capacitor integrators, a floating sampling scheme is devised to decouple the nominal input common-mode voltage and the input DC biasing voltage of the inverter amplifiers, mitigating the limited input CM range. The floating sampling scheme eliminates the need for generating accurate on-chip voltage references by self-referencing the sampling and

integration processes. For the implementation of multi-stage noise-shaping architectures, a floating correlated double sampling technique is proposed by interleaving two sets of capacitors in the switched-capacitor integrator to improve the gain-linearity performance of the inverter amplifiers.

Several 4^{th}-order inverter amplifier-based MASH prototypes with/without the CDS circuit were implemented in a 0.13 μm CMOS process. The CDS-enhanced MASH prototype achieves 71 dB peak SNDR over 20 KHz signal bandwidth, and consumes 18μW power from a 1.5 V supply. The 2^{nd}-order delta-sigma modulator of the first stage achieves 73 dB peak SNDR over 10 KHz signal bandwidth, and consumes 10μW power. The results demonstrates the power efficiency and design flexibility of the inverter amplifier-based design methodologies, which can also be extended for other low power, low cost, and high yield IC applications.

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I. INTRODUCTION

Delta-sigma analog-to-digital converters (ADC) have found widespread applications in high fidelity audio system, fractional-N frequency synthesizer, high precision image sensors, and many other electronic devices [Moon05, Perrott02, and Chae10]. In comparison to other ADC architectures, such as dual slope integrating ADC, flash ADC, pipeline ADC, and successive approximation (SAR) ADC, delta-sigma ADC requires no digital calibration in most implementations, and simple anti-aliasing filters may be used. In addition, the resolution of delta-sigma ADC can be adapted easily by adjusting the sampling frequency according to different applications and operation modes. Due to the inherent memory effect of delta-sigma modulators, however, there is no one-to-one correspondence between the analog input sample and digital output bit(s) as in other ADC architectures. Therefore, a delta-sigma ADC may be reused in an event-based manner rather than cycle-by-cycle time-interleaving in a multi-channel system.

The delta-sigma ADC design will be used in a 1024 channel neural recording IC that includes a 16 x 16 array of these ADCs. Fig. 1.1 shows the system diagram of the high density neural implant (HDNI) currently under development at the Biomimetic group of UCSB. Due to the non-invasive requirement for the HDNI, inductive coupling will be utilized to transmit power from a nearby battery-powered power coil to an on-chip power coil, which is connected to the implant. In addition, the power consumption of the HDNI needs to be very low in order not to affect the neural cells in the ambient environment. Therefore, the total power budget for the HDNI, which

is allocated among pre-amplifiers, channel-select engine, ADC array, wireless transmitter, and digital circuits, should be less than 10 mW, and the power consumption of the ADC needs to be in the micro-watt range. Due to the high density nature of the implant, the ADC also needs to be very area efficient.

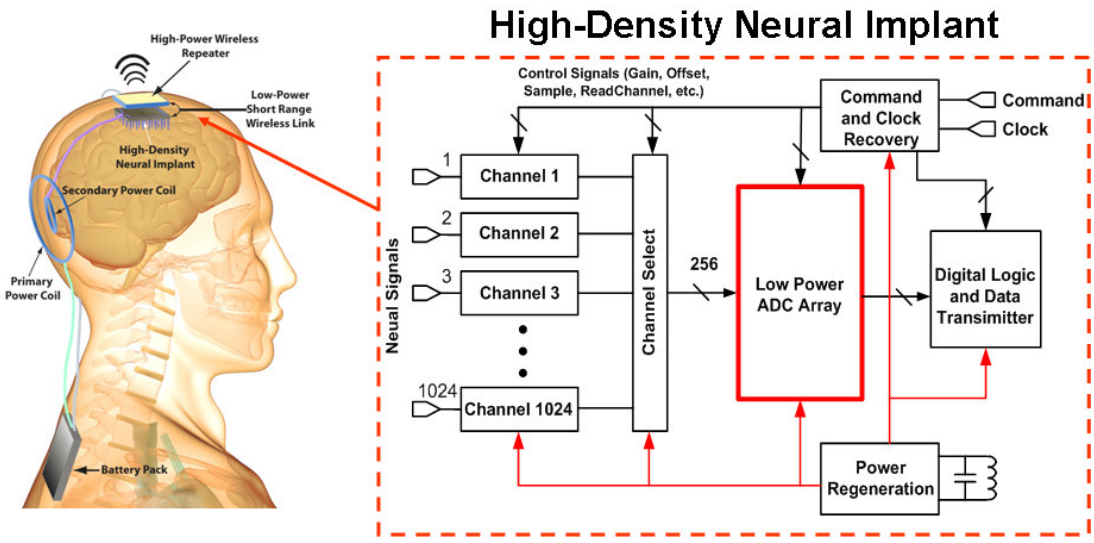


Figure 1.1: System diagram of the high density neural implant

A. Motivation

Over the years, there has been extensive research conducted on the delta-sigma ADC to further improve its resolution, signal bandwidth, and power efficiency. To achieve higher resolution, the multi-stage noise shaping architecture (MASH) has been demonstrated [Matsuya87], which cascades two or more stages of first and/or second order single-loop delta-sigma modulators to achieve higher order noise

shaping through cancellation. Since the signal flow from the first stage to other stages is unidirectional, the overall stability margin in MASH architectures is of the lower order feedback systems. This topology usually requires high gain operational amplifiers (Opamp) to enhance the matching accuracy between the analog loop filter and digital cancellation logic, implying higher power consumption and system complexity. To enable the use of a low gain Opamp in MASH architectures, the sturdy-MASH architecture [Maghari09] feeds the second stage output back into the first stage at its output node to achieve the desired noise cancellation. By eliminating the digital cancellation logic, this approach mitigates the Opamp gain requirements. Since the signal flow between the upper and lower stages becomes bi-directional, however, stability may be an issue in the sturdy-MASH modulator. To extend the signal bandwidth, continuous time (CT) delta-sigma ADC can be employed to replace the switched-capacitor (SC) circuits, thus relaxing the settling requirement for the Opamp and enhancing the overall operation speed of the ADC [Vijay09]. But the fabrication resolution for on-chip resistors severely limits the coefficient accuracy of the loop filters, and additional tuning circuitry are usually required. In addition, the coefficient inaccuracy of CT delta-sigma ADC also prevents its use in the MASH architectures. To lower the power consumption of the ADC, switched-Opamp architecture was proposed [Steyaert94] to turn off the Opamp in the switched-capacitor circuits during sampling phase and turn it on during integration phase. By eliminating the floating switches in the signal path, this approach allows low voltage operation and achieves high power efficiency for the ADC. However, the Opamp is

turned on and off periodically, and the settling time of the resulting transients limits the operation speed. To achieve both low voltage and high speed operation, various IC solutions, such as reset-Opamp [Bidari99], switched-RC [Ahn05], and switched-R-MOSFET-C [Kurahashi07], have been proposed. By avoiding the use of voltage boosting or bootstrapping techniques, these low voltage solutions are compatible with sub-micron CMOS processes and realizes low power consumption for the ADC. To further boost the power efficiency of the ADC, double sampling technique [Kim08] utilizes the Opamp during both sampling and integration phases by including an additional set of sampling capacitor and switches, which allows lower static current for the Opamp. But this arrangement also increases the input-referred KT/C noise and overall silicon overhead.

Aside from those techniques, we also noticed a recent research thrust in literature in developing inverter amplifiers-based SC circuits [Han09, Van08]. In an inverter-based design, the inverter serves as an active feedback element and its transition region is utilized for amplification. The simplicity and versatility of the inverter make this solution attractive and promising. In modern CMOS processes, however, the DC gain of conventional push-pull inverter amplifiers is merely 20-30 dB, rendering it incompetent for high-resolution analog applications. Furthermore, the single-ended nature of the inverter necessitates the use of pseudo-differential structures to increase the dynamic range and common-mode noise rejection, which complicates the overall system design.

In this dissertation, a suite of novel self-biased inverter amplifiers are proposed: the super inverter, the new inverter, and the high-gain inverter. By responding to the differential-mode (DM) signal and common-mode (CM) noises in different ways, all the three inverter amplifiers achieve high DM gain, low CM gain, high supply noise rejection, and fully differential operation. Through employing the self-biasing technique, these inverter amplifiers also show high power efficiency, mismatch tolerance, small form factor, and scalability for different technology nodes. Due to the different operation principles of these inverter amplifiers, they also differ from each other in various aspects such as gain, bandwidth, static current, and linearity performances. Therefore, these inverter amplifiers can be optimally utilized in SC circuits for different applications and design requirements. All the three inverter amplifiers in the dissertation were designed by Prof. Theogarajan, while the modeling, sizing, layout, and chip testing were done by the author.

Furthermore, a floating correlated double sampling (CDS) scheme has been devised to improve the gain-linearity performance of the inverter amplifiers for the implementation of MASH architecture. The floating CDS technique greatly enhances the matching accuracy between the analog loop filter and digital cancellation logic, lowers the in-band noise floor, and suppresses both even and odd order harmonic distortions. Therefore, additional design freedom is attained for choosing between the high-gain inverter amplifier (high gain, high linearity, and high power consumption) without CDS and the low-power inverter amplifiers (low gain, low linearity, and low power consumption) with CDS. To demonstrate the design methodology, these

inverter amplifiers have been implemented in a prototype 2^{nd}-order delta-sigma modulator and 4^{th}-order MASH architectures fabricated in a 0.13 μm CMOS process. Chip measurements show promising results, clearly demonstrating the efficiency and flexibility of the proposed inverter amplifier-based SC circuits for delta-sigma modulation.

B. Organization

The dissertation is organized in the following manner: chapters II, III, IV review the relevant circuit and system-level considerations in the delta-sigma ADC design. Chapters V, VI, VII, and VIII present the inverter amplifier-based design methodology, implementation details, and measurement results. Chapter VIII concludes the whole dissertation.

Chapter II starts with the explanation of the first order delta-sigma modulator to gain an intuitive understanding, and then extends to higher order loop dynamics to reach a general conclusion. The design of the decimation filter, which is an indispensable part of all delta-sigma ADCs, will also be briefly reviewed.

Chapter III describes the circuit-level nonideal effects that affect the achievable performance of the delta-sigma ADC. These nonidealities need to be understood before new circuit topologies or system architectures can be innovated.

Chapter IV compares the system architectures of delta-sigma ADCs in various perspectives. From these comparisons, the advantages and disadvantages of each topology can be identified, and the modulator topology can be tailored for different applications and design targets.

Chapter V presents the self-biased inverter amplifier topologies and floating CDS technique. The operation principles of these inverter amplifiers will be investigated at both large-signal and small-signal levels. The pros and cons of each inverter amplifier will be discussed and compared, and the design guidelines will also be given. The second part of this chapter explains the floating CDS technique in detail.

Chapter VI demonstrates the additional implementation details of both the 2nd order delta-sigma modulator and 4th order MASH architectures at the system, circuit, and layout levels.

Chapter VII discusses the testing setup and measurement results.

Chapter VIII summarizes the contributions of the dissertation and provides future directions.

II. OVERVIEW OF DELTA-SIGMA ADC

A. Delta-Sigma Modulator

Basically, the delta-sigma modulator is a nonlinear feedback system, which forms a low-pass filter for the input signal and a high-pass filter for the quantization noise [Spang62]. The separation of signal and quantization noise in frequency domain enables the use of digital filters in the following to remove the high-pass filtered quantization noise, and therefore a high resolution ADC can be realized with a coarse quantizer. In most feedback systems, a high gain active element at the signal band is inserted into the loop, and the feedback tends to desensitize the nonidealities of the active element and achieve accurate signal processing. Hence, a relatively low performance amplifier can be employed to achieve high resolution data conversion in delta-sigma modulators, while the performance of the Opamps in other ADC architectures directly limits the achievable resolution due to the open-loop structures.

1. First order loop dynamics

Fig. 2.1 shows the system diagram of the 1st-order discrete-time (DT) delta-sigma modulator. The sampled input is fed into an integrator, which is usually realized with a SC integrator in the DT implementations or an active-RC integrator in the CT implementations. For an ideal integrator, its DC gain is infinity since the output of the integrator under DC excitation keeps increasing and never reaches the steady-state. As the signal frequency increases, the gain of the integrator drops since the sampled

input is varying with time and the steady-state output has finite swing. Basically, the integrator is a high gain active element at baseband and it can serve as the loop filter in delta-sigma modulators. The output of the integrator feeds into a low resolution quantizer, usually single-bit in many implementations, to generate the digital outputs. The digital output contains both the signal and the quantization noise, which will be fed back to the modulator input for the next integration. Intuitively, the delta-sigma modulator behaves like a unity-gain amplifier for the input signal, and the digital output follows the analog input in both amplitude and frequency. On the other hand, the high gain active element is located in the feedback path for the quantization noise transfer function, so the noise transfer function of the delta-sigma modulator becomes a high-pass filter.

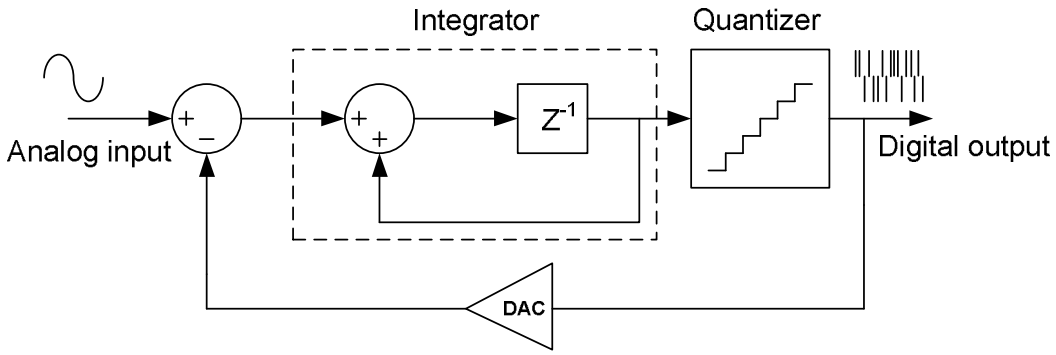


Figure 2.1: System diagram of the 1st order delta-sigma modulator

To gain more insight, the 1st order loop dynamics also needs to be analyzed in a quantitative manner. Firstly, the quantization noise needs to be expressed in a mathematical form. Fig. 2.2 shows a typical ADC transfer curve and the quantization

error under linear excitation. The cyan curve is an ideal ADC transfer curve with infinite resolution. The red curve is an actual ADC transfer curve with finite resolution. The step in the red curve represents the quantization level Δ of the ADC, and the difference between the two curves gives the quantization noise or error, represented by a sawtooth waveform swinging between Δ/2 and –Δ/2. Assuming the input signal is busy, the quantization error Q_e can be treated as a random variable with constant probability density between Δ/2 and –Δ/2. Therefore, the power of the quantization error $Q_e{}^2$ can be calculated as follows. In Eq. 2.2, V_{ref} and N refer to the reference voltage and bits of resolution of the quantizer, respectively.

$$Q_e^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} x^2 dx = \frac{\Delta^2}{12} \tag{2.1}$$

$$\Delta = \frac{V_{ref}}{2^N} \tag{2.2}$$

Fig. 2.3 shows a fictitious continuous waveform of the quantization noise by drawing a straight line between each pair of successive points on the discrete waveform of the quantization noise. Obviously, the power of this continuous waveform is $\Delta^2/12$ and its bandwidth is much wider than the sampling frequency f_s of the quantizer. Since the quantizer is basically a sampled data system, the actual quantization noise waveform is a sampled version of this continuous waveform. Due to noise folding, the high frequency noise power will be aliased down to the baseband, and the total in-band power of the quantization noise is $\Delta^2/12$ with a flat power spectral density (PSD) from DC to $f_s/2$ [Bennett48].

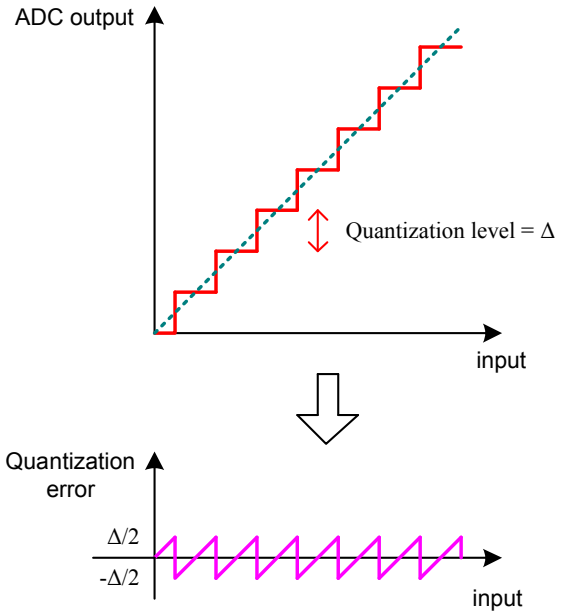


Figure 2.2: ADC transfer curve and the quantization error

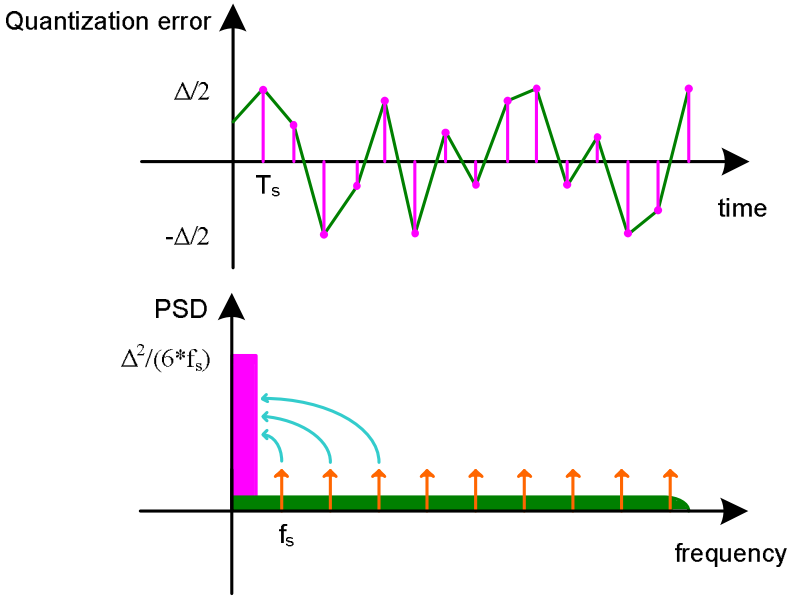


Figure 2.3: Quantization noise waveform and in-band power spectral density

It is well-known that the in-band quantization noise is reduced if the input signal is sampled at a higher frequency than the Nyquist rate f_n. Fig. 2.4 shows the comparison between the Nyquist rate sampling and oversampling. The reason why oversampling reduces the in-band quantization noise is due to a more profound physics behind many phenomena: the averaging effect [Papoulis04]. For example, the flicker noise of a Metal-Oxide-Semiconductor (MOS) device can be reduced by proportionally increasing its W and L, and the larger area tends to smooth the surface states of the channel. For a full-scale sinusoidal input, the maximum signal to quantization noise ratio (SNR) of an oversampling ADC is given by:

$$Q_e^2 = \frac{\Delta^2}{12 \times OSR} \tag{2.3}$$

$$SNR_{\max} = 6.02 \times N + 1.76 + 10 \times \log_{10}(OSR) \tag{2.4}$$

In Eq. 2.3, OSR is the ratio of the sampling frequency to the nominal Nyquist rate. It can be seen that the SNR of an oversampling ADC increases by 3 dB or 0.5 bit for every doubling of the sampling frequency, as illustrated in Fig. 2.5.

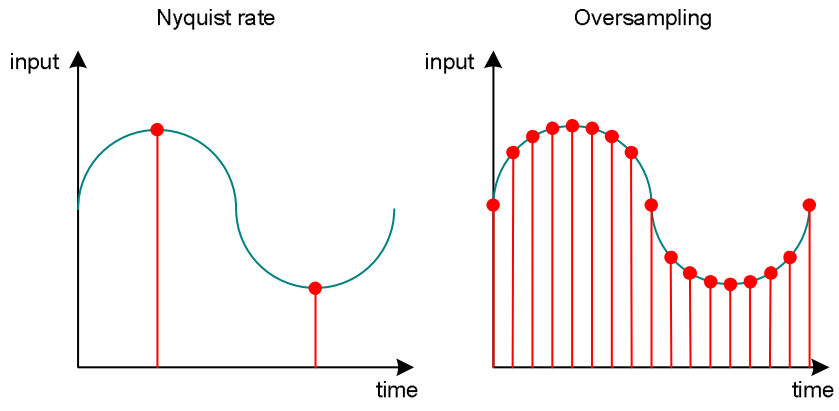


Figure 2.4: Nyquist rate sampling versus oversampling

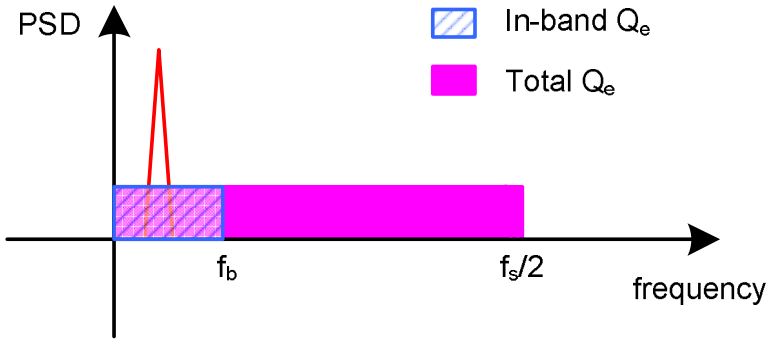


Figure 2.5: Power spectral density of an oversampling ADC

For a coarse quantizer, however, the required sampling frequency would be unrealistically high to achieve reasonable resolution. By high-pass filtering the quantization noise using a delta-sigma modulator, the requirement on the sampling frequency can be greatly reduced. Fig. 2.6 shows the simplified model of the 1st-order delta-sigma modulator. From this model, its signal transfer function STF and noise transfer function NTF can be found, given by:

$$STF(Z) = \frac{Y}{X} = Z^{-1} \tag{2.5}$$

$$NTF(Z) = \frac{Y}{Q_e} = 1 - Z^{-1} \tag{2.6}$$

In the Z-domain, the STF is a clock cycle delay, and the NTF is a differentiator. To find the in-band quantization noise of the 1st-order modulator, the power of the noise transfer function $|NTF(Z)|^2$ will be integrated from DC to the Nyquist frequency [Johns97]. Then, the maximum SNR under both oversampling and 1st-order noise shaping can be estimated, as shown in Eq. 2.7 and 2.8. It is seen that the maximum

SNR of the 1st-order modulator increases by 9 dB or 1.5 bits for every doubling of the sampling frequency, as illustrated in Fig. 2.7.

$$Q_e^2 = \frac{\Delta^2 \pi^2}{36 \times OSR^3} \tag{2.7}$$

$$SNR_{\max} = 6.02 \times N + 1.76 - 5.17 + 30 \times \log_{10}(OSR) \tag{2.8}$$

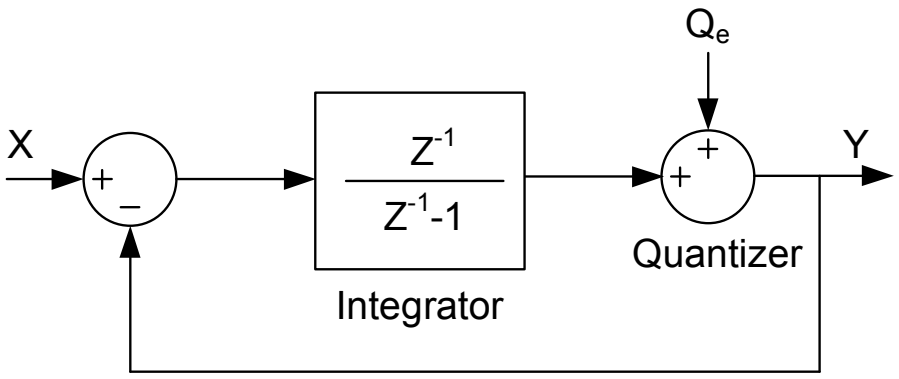


Figure 2.6: Simplified model of the 1st-order delta-sigma modulator

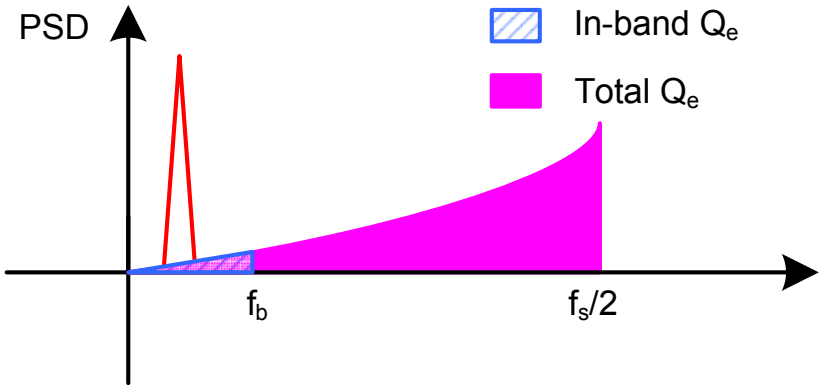


Figure 2.7: Power spectral density of the 1st-order delta-sigma modulator

2. Higher order loop dynamics

To achieve more noise shaping, higher order delta-sigma modulator can be built. Basically, a higher order loop filter tends to have sharper transition from its pass band to stop band than a lower order filter, and more quantization noise can be moved to high frequency band. In the higher order modulator, more integrators are cascaded in a loop, and the number of the integrators determines the order of the system since each integrator contributes a DC pole.

Fig. 2.8 shows a simplified model of the 2^{nd}-order DT delta-sigma modulator [Boser88]. The attenuation factor G_1 is added to limit the voltage swing at the input of the first integrator since the feedback takes two clocks cycles. Without the attenuation, the integrator output will saturate even for a small input, and the effective gain of the amplifier in the integrator will drop, degrading the performance of the loop filter. More about the finite gain effect will be discussed in the next chapter. G_2 and G_3 are chosen to attain the desired STF and NFT. G_c represents the effective gain of the quantizer, as illustrated in Fig. 2.9. For a single-bit quantizer, its gain is not well defined and dependent on the average input amplitude of the quantizer. Since the output of the modulator follows the input through the feedback, G_c must satisfy that $G_1G_2G_c=1$, statistically [Baker08]. For a single-loop delta-sigma modulator, G_c is embedded in the loop transmission so it is not important. For a MASH modulator, however, G_c is critical for precisely extracting the quantization noise. Otherwise, the accuracy of the noise cancellation would drop greatly. Eq. 2.9 and 3.0 show the STF and NTF of the 2^{nd}-order delta-sigma modulator. Given that

$G_1G_2G_c=1$ and $G_{1,2,3}$ are chosen properly, the STF and NTF can simplified as shown in Eq. 3.1 and 3.2.

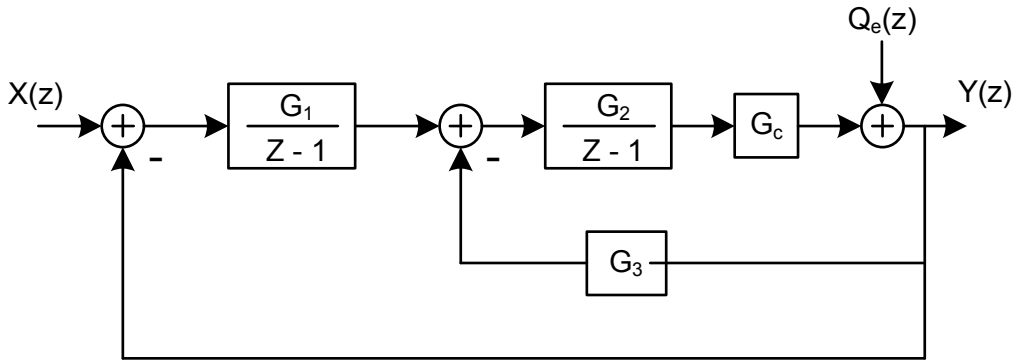


Figure 2.8: Simplified model of the 2nd-order delta-sigma modulator

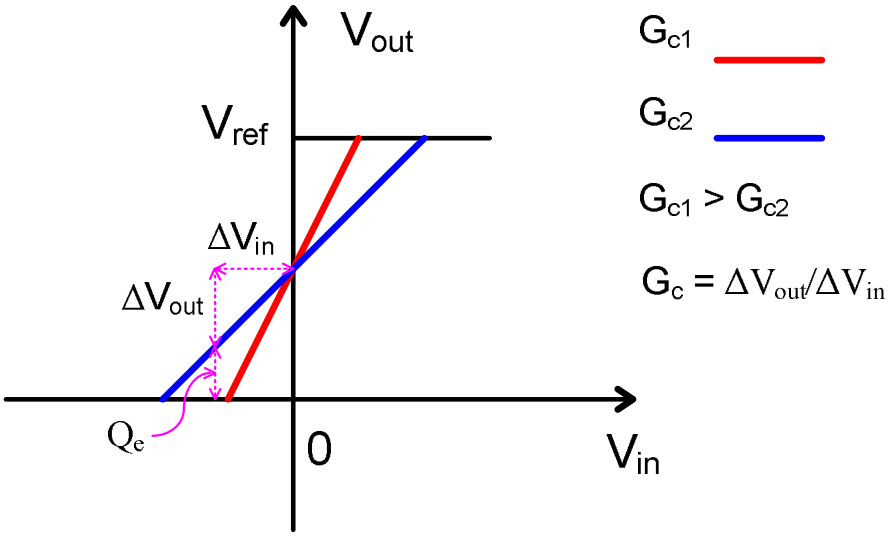


Figure 2.9: Transfer curve of a single-bit quantizer

$$STF = \frac{G_1 G_2 G_c}{(Z-1)^2 + G_2 G_3 G_c (Z-1) + G_1 G_2 G_c} \tag{2.9}$$

$$NTF = \frac{(Z-1)^2}{(Z-1)^2 + G_2 G_3 G_c (Z-1) + G_1 G_2 G_c} \tag{2.10}$$

$$STF = Z^{-2} \tag{2.11}$$

$$NTF = (1 - Z^{-1})^2 \tag{2.12}$$

It's clear that the STF is a two clock cycle delay and the NTF is a 2nd-order high-pass filter. Using the same method, the in-band quantization noise and maxim SNR of the 2nd-order delta-sigma modulator can be derived as given in Eq. 2.13 and 2.14. For the 2nd-order modulator, the PSD of the shaped quantization noise increases at a rate of 40 dB per decade, while it is 20 dB per decade for the 1st-order modulator. In addition, the maximum SNR increases by 15 dB or 2.5 bits for every doubling of the sampling frequency.

$$Q_e^2 = \frac{\Delta^2 \pi^4}{60 \times OSR^5} \tag{2.13}$$

$$SNR_{\max} = 6.02 \times N + 1.76 - 12.19 + 50 \times \log_{10}(OSR) \tag{2.14}$$

The in-band quantization noise and maximum SNR can be generalized for any Lth-order delta-sigma modulators, given by Eq. 2.15 and 2.16. In general, the maximum SNR of the Lth-order modulator increases by 3(2L+1) dB or (L+0.5) bits for every doubling of the sampling frequency, as shown in Fig. 2.10. In reality, there are many circuit nonidealities, such as KT/C noise, greatly limiting the achievable resolution. Furthermore, L<4 usually needs to be satisfied in a single-loop delta-sigma modulator for the stability consideration. To achieve higher order (L>=4) noise shaping, MASH

architectures will be exploited instead. Some advanced topics of delta-sigma ADCs will be investigated in the following chapters, and the core of the dissertation is also unveiled.

$$Q_e^2 = \frac{\Delta^2}{12} \cdot \frac{\pi^{2L}}{(2L+1) \times OSR^{2L+1}} \tag{2.13}$$

$$SNR_{\max} = 6.02N + 1.76 - 10\log_{10}\left(\frac{\pi^{2L}}{2L+1}\right) + (2L+1) \times 10\log_{10}(OSR) \tag{2.14}$$

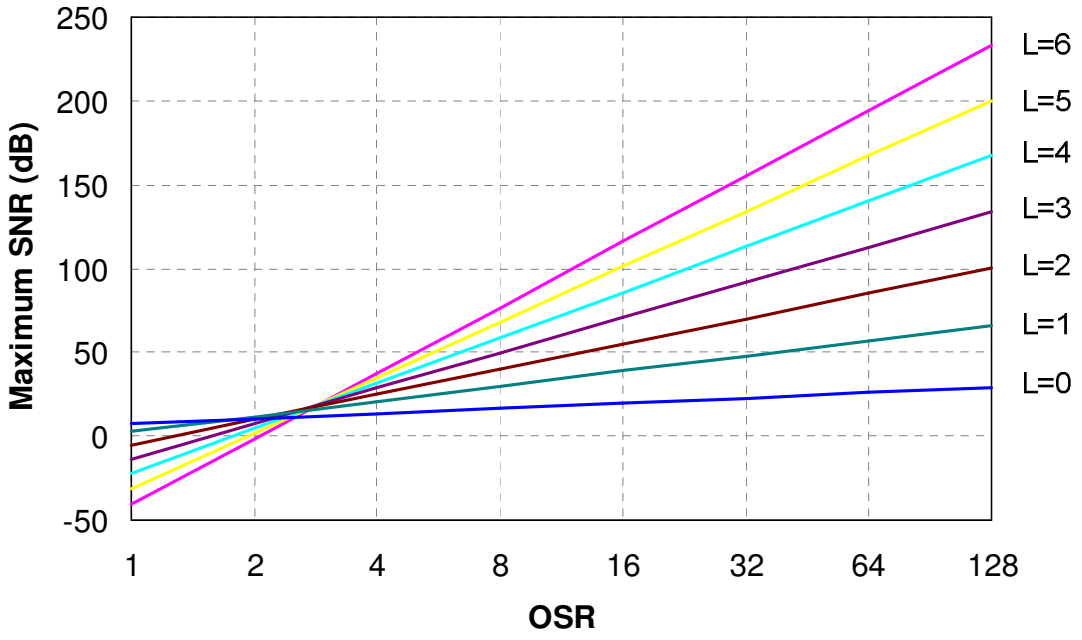


Figure 2.10: Maximum SNR versus OSR

B. Decimation Filter

At the output of the delta-sigma modulator, analog input signal has been converted into low-resolution digital outputs. Although the quantization noise is moved to high frequency, it is still in the output bits. Hence, the other part of the delta-sigma ADC design is to build the digital decimation filter, which filters out the high frequency quantization noise and converts the coarse binary bits into high resolution digital outputs. In this section, the design of the decimation filter will be briefly reviewed, completing the introduction of the delta-sigma ADC.

Intuitively, the decimation filter calculates the running averages of the incoming digital bits from the delta sigma modulator. After the decimation filter, the low frequency components are retained, but the high frequency quantization noise has been removed. The digital outputs are also down-sampled to the Nyquist rate for further signal processing.

Eq. 2.15 shows the transfer function of a typical running-average filter, with a decimation ratio of M. The pole and zero locations for M=8 are plotted in the Z-plane, and the frequency response can be found by moving around the unity circle, as shown in Fig. 2.11. Clearly, it has the low-pass filtering characteristics. Since the frequency response looks like a comb from DC to the sampling frequency, it's also known as the comb filter.

$$H(Z) = \frac{(1 + Z^{-1} + Z^{-2} + \cdots + Z^{-(M-1)})}{M} = \frac{1}{M} \cdot \left(\frac{1 - Z^{-M}}{1 - Z^{-1}} \right) \tag{2.15}$$

In the decimation filter, multiple running-average filters are cascaded and organized in a power-efficient form, as illustrated in Fig. 2.12. The cascade stages usually need to be higher than the order of the preceding modulator to achieve sufficient out of band rejection [Candy86].

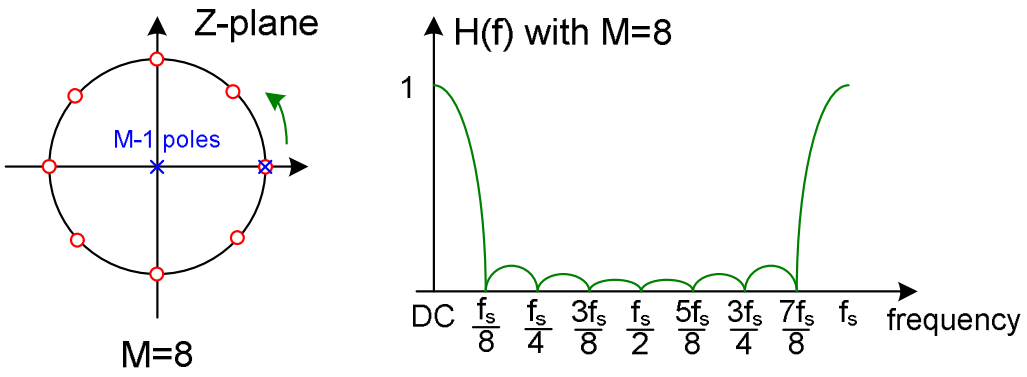


Figure 2.11: Running-average filter with M=8

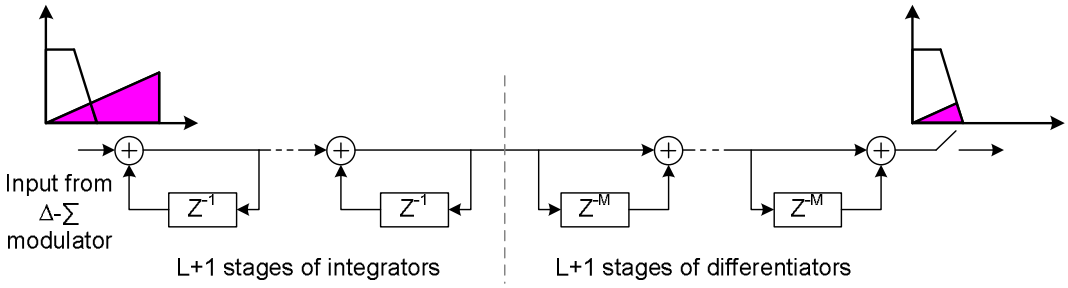


Figure 2.12: Part of the Decimation filter – $Sinc^{L+1}$ FIR filter

III. CIRCUIT CONSIDERATIONS

In this chapter, common circuit nonidealities that limit the achievable performance of the delta-sigma ADC will be discussed in different perspectives: Opamp nonidealities, noise, and distortion. Those issues are critical in understanding the different system architectures of the delta-sigma ADC, so this chapter precedes the system discussions. In many high-speed applications, the quantizer nonidealities, such as comparator hysteresis, metastability, and delay, also affect the resulting SNR. Due to the low frequency operation of this design, the discussion of those issues will be omitted for simplicity.

A. Opamp Nonidealities

In both DT and CT delta-sigma modulators, Opamp serves as the active feedback elements in the loop filter. It affects the performance of the delta-sigma modulator in many aspects: integrator leakage, flicker noise and DC offset, harmonic distortion, and matching accuracy of the loop filters. Furthermore, it also dominates the power consumption of the modulator due to the static current.

1. Finite gain effect

Due to the limited transconductance (g_m) and output resistance (r_o), any Opamp has finite DC gain ranging from 20 dB to 100 dB, which causes degradations in the low frequency noise shaping and matching accuracy of the loop filters. Fig. 3.1 shows a single-ended SC integrator and the associated timing diagram of the clock signals.

During the integration phase, the potential at the virtual ground, V_x, is initially pushed down to $-V_i[n]$ due to the feedthrough effect of C_s, then the negative feedback around the Opamp asymptotically pulls V_x back to ground potential. For an ideal Opamp with infinite gain, the steady-state value of V_x is zero, and all the charges on C_s will be completely transferred to C_f. For a practical Opamp with finite gain of A, V_x would settle at $-V_o[n+1]/A$ instead, and a fraction of the charges on C_s leak away. The integrator leakage effect moves the pole of the integrator away from DC, thus levels off the shaped quantization noise in the baseband.

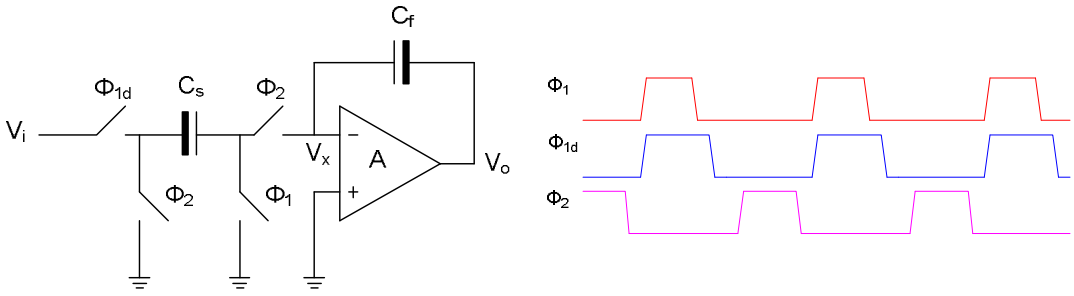


Figure 3.1: A delaying switched-capacitor integrator

To quantify the leakage effect, the integrator transfer function with finite Opamp gain of A can be found by applying the charge conservation for both sampling and integration clock phases. As shown in Eq. 3.1 and 3.2, the pole of the integrator moves away from DC (Z=1) to $Z=1-(C_s/C_f)/A$ inside the unity circle. The DC gain of the integrator also becomes A, instead of infinity. Eq. 3.3 gives the first order NTF considering the integrator leakage effect, and Fig. 3.2 shows the Z-plane root locus of the NTF. The -3dB corner frequency of the NTF can be found by applying bilinear transform [Johns97], which is given in Eq. 3.4. Fig. 3.3 compares the frequency

responses between an ideal NTF and a practical NTF considering the integrator leakage.

In order to mitigate the resulting noise notch, it is necessary to keep the corner frequency within the signal bandwidth, as shown in Eq. 3.5. As a sanity check, A=OSR gives 0.2 dB additional noise, thus the integrator leakage effect is rarely serious. In most delta-sigma ADCs, the nominal OSR ranges from 64 to 256, thus the required Opamp gain needs to be around 40-50 dB. This can be easily achieved given today's amplifier design techniques, and the Opamp can be optimized for higher power efficiency or other performance targets. In general, it's acceptable to have an Opamp of A=OSR in the delta-sigma modulator design.

$$C_s V_i[n] + C_f V_o[n]\frac{1+A}{A} = C_s V_o[n+1]/A + C_f V_o[n+1]\frac{1+A}{A} \tag{3.1}$$

$$\frac{V_o(Z)}{V_i(Z)} = \frac{C_s}{C_f}\frac{1}{Z\left[1+\left(1+\frac{C_s}{C_f}\right)\cdot\frac{1}{A}\right]-\left(1+\frac{1}{A}\right)} = A\,@\,DC \tag{3.2}$$

$$NTF(f) \approx 1-(1-\frac{C_s}{C_f}\cdot\frac{1}{A})Z^{-1} \tag{3.3}$$

$$\omega_{-3dB} \approx \frac{C_s}{C_f A} \text{ rad/sample} \tag{3.4}$$

$$\frac{C_s}{C_f A} < \frac{\pi}{OSR} \Rightarrow A > \frac{C_s}{C_f}\frac{OSR}{\pi} \Rightarrow \boxed{A = OSR} \tag{3.5}$$

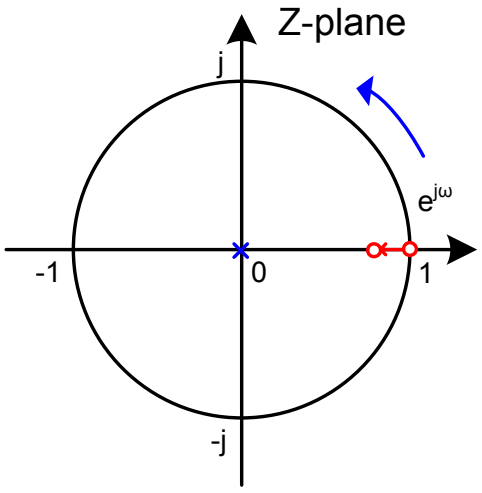


Figure 3.2: Root locus of the 1st order NTF

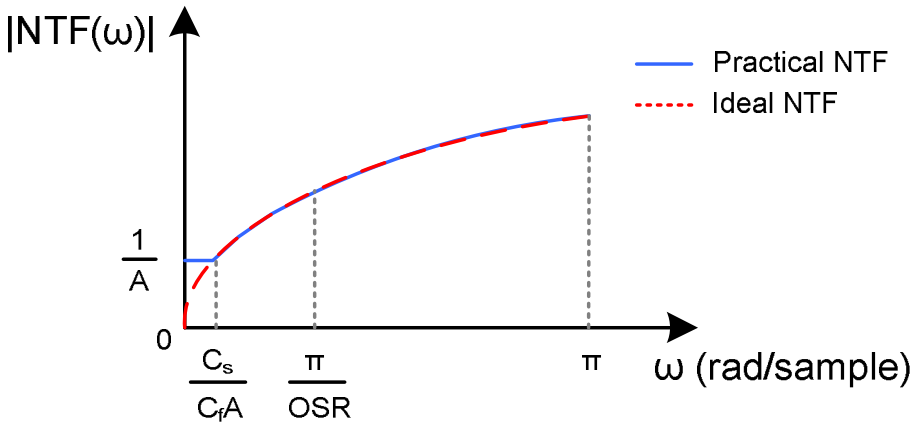


Figure 3.3: Frequency response of the 1st order NTF

In the MASH architectures, however, much higher Opamp gain is often required to enhance the matching accuracy between the analog and digital signal paths. Finite Opamp gain changes the pole locations of the NTF and modifies the absolute gain factor of the integrator. The transfer function of a SC integrator with finite Opamp gain of A is rewritten in Eq. 3.6, 3.7 and 3.8, where a and D represent the nominal value and relative error of the integrator gain (C_s/C_f), respectively.

$$H(Z) = \frac{V_o(Z)}{V_i(Z)} = \frac{a'}{Z - p'} \tag{3.6}$$

$$a' \approx a\left[1 - D - (1+a)/A\right] \tag{3.7}$$

$$p' \approx 1 - \frac{a}{A} \tag{3.8}$$

Fig. 3.4 shows a typical two-stage MASH architecture, where E_1 is cancelled through the matching between NTF_1H_1 and STF_2H_2. H_1 and H_2 are built with digital filters, and thus have ideal transfer functions. NTF_1 and STF_2 are analog filters, which will be affected by circuit nonidealities. To quantify the first order noise leakage, two assumptions are made: 1. STF_2 is an ideal function; 2. NTF≈1/H(Z) [Schreier04]. Eq. 3.9 clearly shows that there will be an unfiltered component approximately equal to E_1/A, and a first-order-shaped component dominated by the capacitor mismatching.

$$\begin{aligned} \left|H_{1l}(Z)\right| &= \left|NTF_1H_1 - STF_2H_2\right| \\ &= \left|NTF_1 - H_2\right| \\ &= \left|\frac{Z-1}{a} - \frac{Z-p'}{a'}\right| \\ &\approx \left|\frac{1}{A} + (Z-1)\cdot\left[D/a + (1+1/a)/A\right]\right| \end{aligned} \tag{3.9}$$

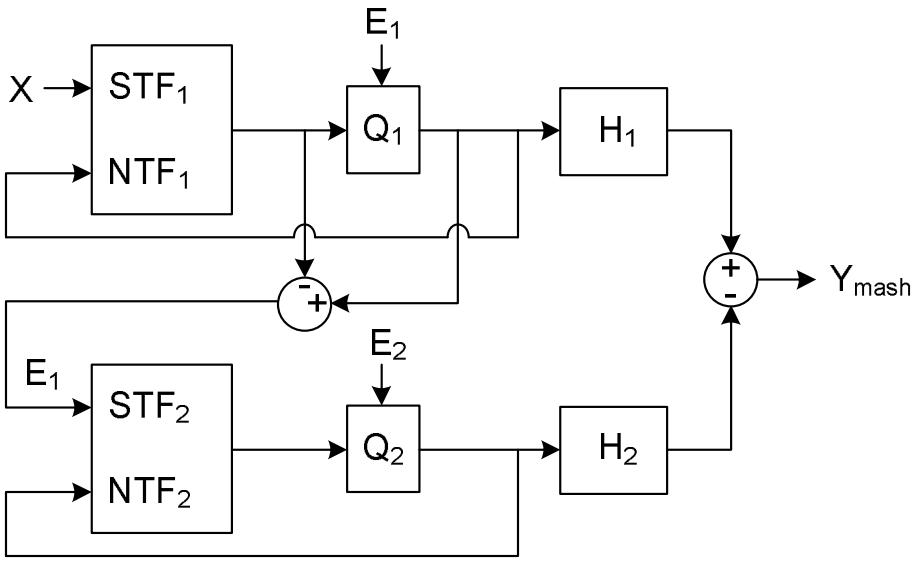


Figure 3.4: Two-stage MASH architecture

To analyze higher order noise leakage, matlab simulation can be utilized. Fig. 3.5 plots the simulated power spectral density (PSD) of a 2-2 MASH architecture assuming Opamp gain of 40, 60, 80, and 100 dB. Only quantization noise is simulated in the simulation, and other noise sources are turned off for clarity. In the overlaid output spectrums, it can be seen that there are an unfiltered leakage component roughly proportional to 1/A, and a second-order-shaped leakage component. Clearly, the mismatch between the filters warps up the in-band noise floor. On the other hand, the high frequency noise spectrum is still dominated by the 4^{th}-order shaped quantization noise E_2. The corner frequency is determined by where the leakage noise spectrum of E_1 meets the shaped noise spectrum of E_2. Intuitively, higher Opamp gain results in lower corner frequency, and hence better SNR possibility.

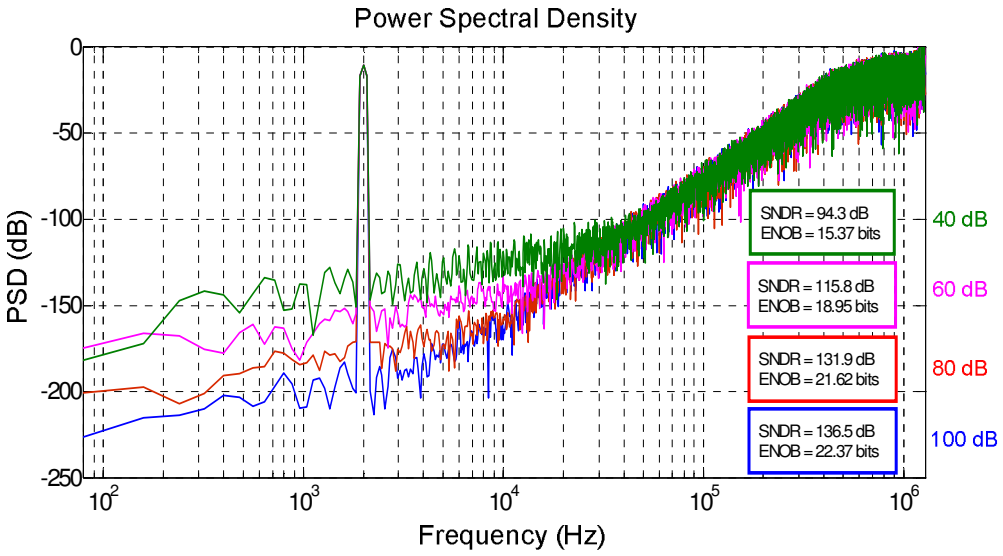


Figure 3.5: Opamp gain effects on the 4th order MASH

2. Settling time

The previous section analyzes the steady-state behavior of the Opamp in the SC integrator, assuming infinite settling speed. During the transient time, any Opamp has finite settling speed due to the limited current available for charging or discharging the loading capacitors. In addition, the settling process of the OPAMP may be linear or nonlinear depending on the input amplitude.

For a small-signal input, the output current of the OPAMP is proportional to the input voltage, and the time constant of the feedback system keeps the same. For a given settling time, the steady-state output voltage will be proportional to the input voltage, corresponding to the linear settling region. For a large-signal input, the output current is limited by the maximally available current in the circuit, and in the given time the stead-state output voltage reaches a constant value, independent of the

input voltage. This corresponds to the nonlinear settling or the slew-rate limiting region. Between these two regions, the output voltage first changes in a slew-rate limiting manner, then the OPAMP enters the small-signal operating mode, and the linear settling takes place for the rest of the period. This corresponds to the weakly nonlinear region. Fig. 3.6 illustrates the three cases of the settling process for different input amplitudes.

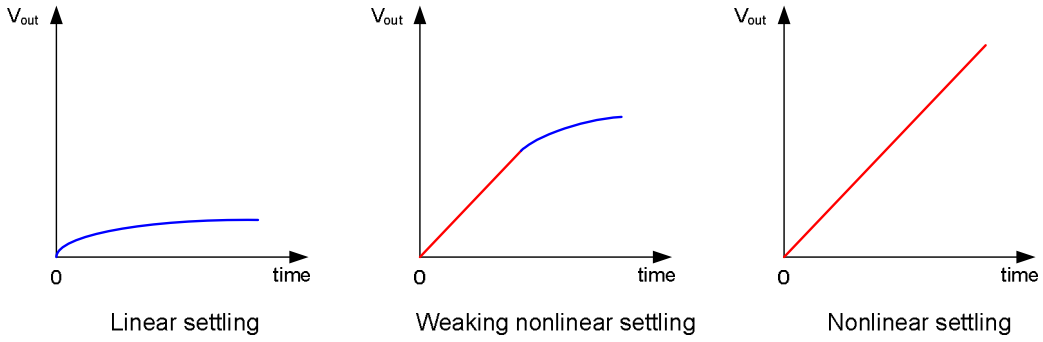


Figure 3.6: Three settling processes for different input steps

During the design phase, it is useful to quantify the time constant for the linear settling. Fig. 3.7 shows the small-signal circuit diagram of a single-ended SC integrator in the integration phase. By applying KCL and KVL, the Laplace-domain transfer function of the feedback system is shown in Eq. 3.10 and 3.11, assuming single-pole rolloff and infinite R_{out} for the amplifier.

$$\frac{V_o}{V_i} = -\frac{C_s}{C_f} \cdot \frac{1 - S\frac{C_f}{g_m}}{1 + S\frac{C_L + C_f(1-F)}{F \cdot g_m}} \tag{3.10}$$

$$F = \frac{C_f}{C_f + C_s + C_p} \tag{3.11}$$

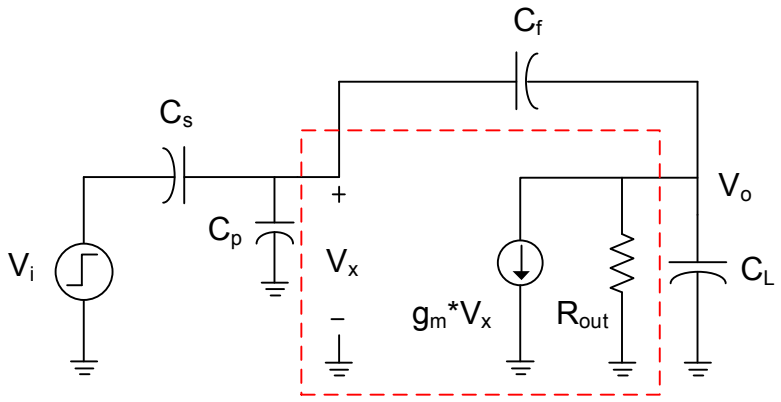


Figure 3.7: Small-signal model of a capacitive-feedback amplifier

In Eq. 3.10, there is a pole determined by the transconductance (g_m) of the amplifier and the effective output capacitance, and a feedthrough zero. For a step input, the circuit response is given in Eq. 3.12 and 3.13.

$$V_{o,step}(t) = -V_{i,step} \cdot \frac{C_s}{C_f}\left\{1-\left(1+\frac{P}{Z}\right)\exp^{-t/\tau}\right\} \tag{3.12}$$

$$P = -\frac{1}{\tau} = -\frac{F \cdot g_m}{C_L + C_f(1-F)}, Z = \frac{g_m}{C_f} \tag{3.13}$$

The "$(1+P/Z)\exp^{-t/\tau}$" term indicates the relative settling error, and it is a constant determined by the bandwidth of the Opamp. The integrator gain error is often tolerable in the design of delta-sigma modulators, but not in the MASH architectures. It has been shown that finite bandwidth also causes the integrator leakage if finite gain effect is included [Sansen99], but that is quite small and can be omitted for hand analysis [Gustavsson00]. As long as the settling is linear, the required settling accuracy can be significantly lower than the accuracy of the delta-sigma ADC.

Therefore, a relatively low speed Opamp may be employed in the delta-sigma ADC for achieving higher power efficiency.

For small input step, the initial rate of change of the output voltage is proportional to the nominal steady-state output voltage: $|V_{o,step}|/\tau$. If it is smaller than the slew rate (SR), linear settling can be assumed for the whole period. For large input step, $|V_{o,step}|/\tau$ may be greater than the SR, then the output voltage changes in a constant rate. If the output voltage reaches a point where $\Delta V/\tau$ equals the slew rate ($\Delta V=|V_{o,step}-V(t)|$), the Opamp would then enter the linear settling region. In case the input step is so large that $\Delta V/\tau$ is always greater than the SR, the Opamp would be in the nonlinear settling region for the whole period [Wooley94]. The three cases are summarized in Eq. 3.14, 3.15, and 3.16, where T_s refers to the given settling time.

$|V_{o,step}| < SR*\tau$ (Linear settling):

$$V_{o,final} = V_{o,step}\left\{1-\left(1+\frac{P}{Z}\right)\exp^{-\frac{T_s}{\tau}}\right\} \tag{3.14}$$

$SR*\tau < |V_{o,step}| < SR(\tau+T_s)$ (Weakly nonlinear settling):

$$V_{o,final} = V_{o,step} - \mathrm{sgn}\left(V_{o,step}\right)\cdot SR\cdot\tau\left(1+\frac{P}{Z}\right)\exp^{-\left(1+\frac{T_s}{\tau}-\frac{|V_{o,step}|}{\tau^2}\right)} \tag{3.15}$$

$|V_{o,step}| > SR(\tau+ T_s)$ (Nonlinear settling):

$$V_{o,final} = \mathrm{sgn}\left(V_{o,step}\right)\cdot T_s\cdot SR \tag{3.16}$$

Fig. 3.8 illustrates the different settling regions in terms of the nominal steady-state output voltage. In order to minimize harmonic distortion, it is important to limit

the input and output voltage swings of the Opamp and keep it from operating in the slew-rate limiting regions.

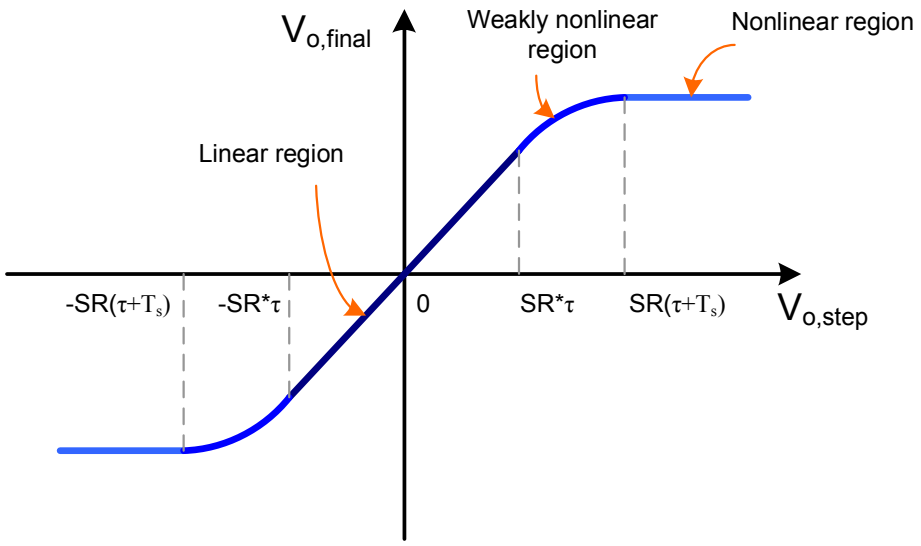


Figure 3.8: Three settling regions in terms of the nominal output voltage

3. Gain nonlinearity

In this section, the amplifier gain nonlinearity will be investigated, and its effects on the in-band noise floor and harmonic distortion of delta-sigma modulators will be highlighted. Fig. 3.9 shows the typical DC transfer curve of an amplifier. When the input/output swing is small, the amplifier is operating in the high gain region. When the input/output swing is large, the output level becomes saturated and the gain of the amplifier will drop. As a result, the low frequency noise notch will be effectively widened and the actual in-band noise floor is raised up.

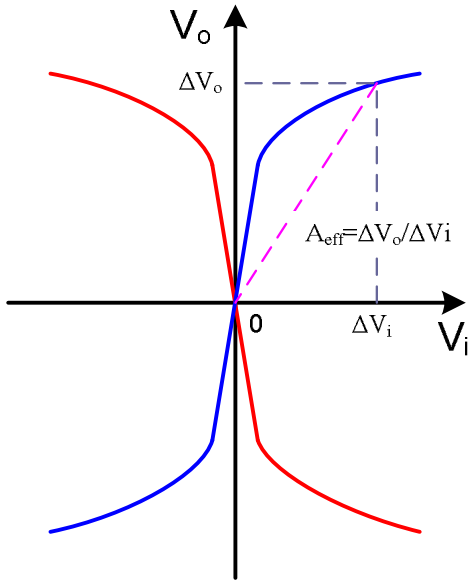


Figure 3.9: Typical amplifier transfer characteristics

Due to the chaotic nature of the delta-sigma modulator, it's nontrivial to find an analytical solution for the nonlinear time-varying problem. To simplify the analysis, the effective gain (A_{eff}) of the amplifier can be defined as the ratio of the maximum output voltage of the SC integrator to the corresponding input voltage of the amplifier. This represents the worst case. The additional quantization noise can be estimated by integrating $|NTF(\omega)|^2 \approx A_{eff}^{-2}+\omega^2$ from DC to π/OSR and comparing the result against the $A_{eff} = \infty$ case. Eq. 3.17 and 3.18 show the derivation. From this simple model, the SNR degradation can be plotted in terms of OSR/A_{eff}., shown in Fig. 3.10. For A_{eff} = OSR, the SNR degradation is only 0.2 dB, as mentioned previously. For A_{eff} < OSR/6, the SNR degradation can be more than 10 dB, which is phenomenal.

$$\Delta Q_e^2 = \int_0^{\frac{\pi}{OSR}} \left(A_{eff}^{-2} + \omega^2 \right) d\omega$$
$$= \frac{\pi}{A_{eff} OSR} + \frac{\pi^3}{3OSR^3} \tag{3.17}$$

$$\Delta SNR = 10 \log_{10} \left(1 + \frac{3OSR^2}{A_{eff}^2 \pi^2} \right) - 1 \tag{3.18}$$

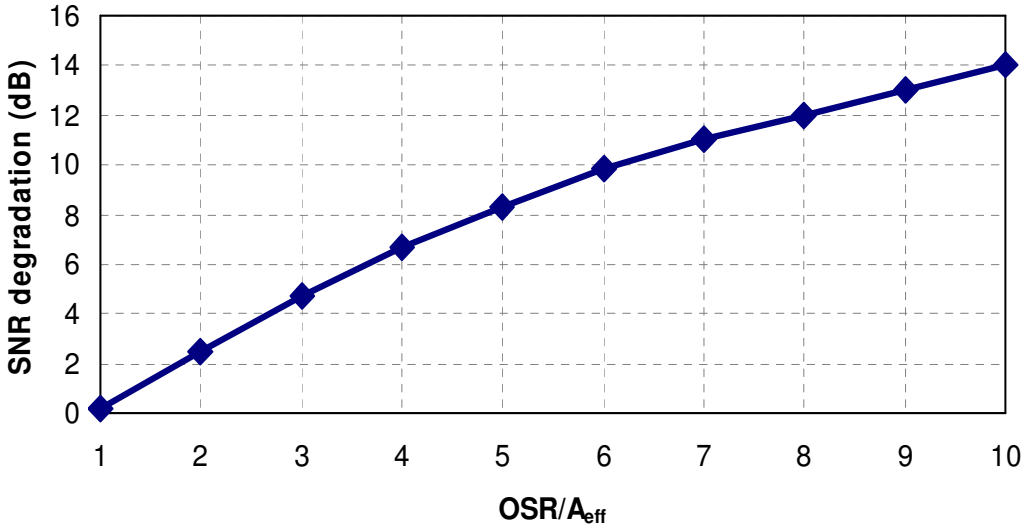


Figure 3.10: SNR degradation and the effective amplifier gain

In addition to raising the in-band noise floor, the amplifier gain nonlinearity also greatly contributes to the harmonic distortion in the SC integrator, which lowers the SNDR (including distortion tones) of the modulator for large input signals. The amplifier' gain characteristics can be approximated using a Volterra series [Yuan01], a hyperbolic tangent (tanh) function [Razavi06], or a variable-gain model [Yavari07]. However, the nonlinear gain estimation in the SC integrator is an iterative recursive procedure, so there is no simple analytical formula relating the harmonic outputs with

the nonlinear gain characteristics of the amplifier. Instead, the nonlinear model of the SC circuits can be implemented in a numerical simulator such as Matlab to estimate the harmonic distortions.

To further simplify the problem, a three-step procedure may be utilized [Yavari07]: first, the nominal output voltage $V_{nom}[n]$ of a SC integrator is predicted using the small-signal DC gain A_0; then, the large-signal DC gain $A_{dc}(V_{nom}[n])$ is calculated based on the predicted output voltage. The relationship between A_0 and $A_{dc}(V_{nom}[n])$ is given in Eq. 3.19 and 3.20, where α and β serve as the curve-fitting parameters in the nonlinear gain model; finally, the actual output voltage $V_o[n]$ of the SC integrator is calculated based on $A_{dc}(V_{nom}[n])$, as shown in Eq. 3.21, 3.22, and 3.23. Fig. 3.11 shows a system-level model of the SC integrator, implementing the above procedures. It is seen that the nonlinear gain characteristics of the amplifier clearly affects the harmonic distortion of the SC integrator, hence the SNDR performance of the modulator.

$$V_{nom}[n] = \frac{1+A_0}{1+a+A_0} V_o[n-1] + \frac{aA_0}{1+a+A_0} V_i[n-1] \tag{3.19}$$

$$A_{dc}\left(V_{nom}[n]\right) = A_0 \left(1 - \alpha \left| \frac{V_{nom}[n]}{V_{o,\max}} \right|^{\beta} \right) \tag{3.20}$$

$$f\left(V_{nom}[n]\right)=\frac{a\cdot A_0\left(1-\alpha\left|\frac{V_{nom}[n]}{V_{o,\max}}\right|^{\beta}\right)}{1+a+A_0\left(1-\alpha\left|\frac{V_{nom}[n]}{V_{o,\max}}\right|^{\beta}\right)} \tag{3.21}$$

$$g\left(V_{nom}[n]\right)=\frac{1+A_0\left(1-\alpha\left|\frac{V_{nom}[n]}{V_{o,\max}}\right|^{\beta}\right)}{1+a+A_0\left(1-\alpha\left|\frac{V_{nom}[n]}{V_{o,\max}}\right|^{\beta}\right)} \tag{3.22}$$

$$V_o[n]=g\left(V_{nom}[n]\right)\cdot V_o[n-1]+f\left(V_{nom}[n]\right)\cdot V_i[n-1] \tag{3.23}$$

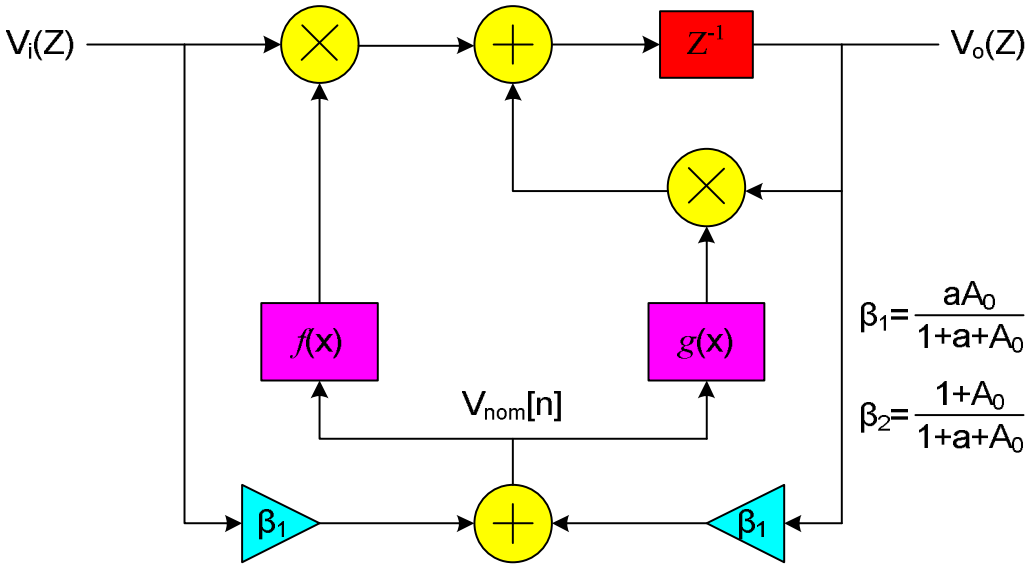


Figure 3.11: Modeling the amplifier gain nonlinearity in a delaying SC integrator

B. Noise Sources

In addition to the quantization noise, there are also other noise sources in the delta-sigma modulator, such as KT/C noise, OPAMP noise, and jitter noise, affecting the achievable SNR performance of the modulator. Due to the possible signal-dependence of the quantization noise, it is important to minimize its contribution to the overall in-band noise power for achieving lower nonlinear distortion. The KT/C and Opamp thermal noise, which have a white spectrum, hence dominate the in-band noise floor for design optimization. Fig. 3.12 shows a typical noise budget in SC-based delta-sigma modulators.

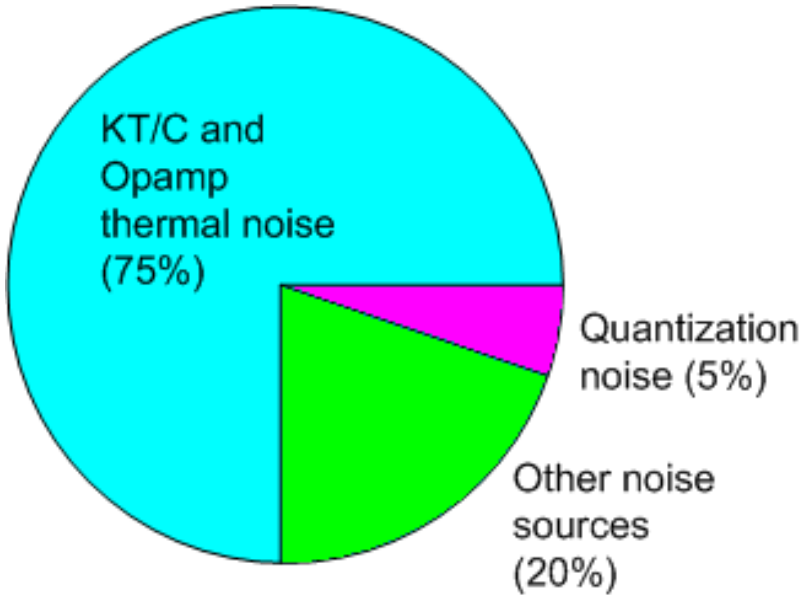


Figure 3.12: Noise budget of the delta-sigma modulator

1. Thermal noise

Due to the Brownian motion of thermally-agitated charge carriers, any electrical conductor, such as a resistor or the conducting channel of a MOS device, exhibits an additive noise voltage at its terminals no matter there is DC current flow or not [Gray04]. In SC circuits, thermal noise manifests itself as the KT/C noise (or the switching noise) and Opamp thermal noise. It is helpful to analyze the noise process and quantify its contribution to the SNR performance of the modulator.

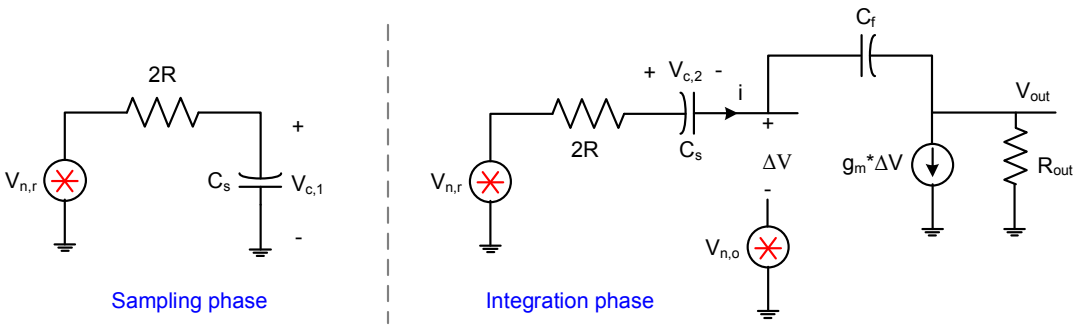


Figure 3.13: Small-signal models for thermal noise calculation

Fig. 3.13 shows the small-signal models for thermal noise calculation in the SC integrator. The conducting channel of a MOS switch is modeled as a resistor R, controlled by the gate-source voltage of the MOS device in the linear mode. It will be shown that the value of R has little effect on the resulting input-referred noise voltage. It's the size of the sampling capacitor (C_s) that determines the in-band noise floor.

During the sampling phase, the SC circuit is modeled as an equivalent first-order RC filter. The noise power of the channel ($\overline{V_{n,r}^2}$) is given by Eq. 3.24. Theoretically, thermal noise has a finite PSD from DC to infinite frequency, implying infinite noise

voltage at the terminals. After considering the filtering effect of the capacitor, it can be shown that the actual noise power on top of the capacitor is independent of the resistance, and occupies a spectrum from DC to the -3dB frequency ($f_{\text{-3dB}}$) of the RC filter, as shown in Fig. 3.14.

In practice, $f_{\text{-3dB}}$ is usually designed 10 times larger than the clock frequency for the SC circuit to achieve sufficient settling accuracy. Due to the inherent noise folding, the sampling process mixes the high frequency noise down to baseband, and the total in-band noise power on top of the capacitor ($\overline{V_{c,1}^2}$) during the sampling phase is therefore equal to KT/C/OSR. Hence, it's called the KT/C noise.

$$\overline{V_{n,r}^2} = 4KT \cdot 2R \cdot \Delta f \tag{3.24}$$

$$\overline{V_{c,1}^2} = 4KT \cdot 2R \cdot \frac{\pi}{2} \cdot \frac{1}{2\pi \cdot 2RC} \cdot \frac{1}{OSR} = \boxed{\frac{KT}{C \cdot OSR}} \tag{3.25}$$

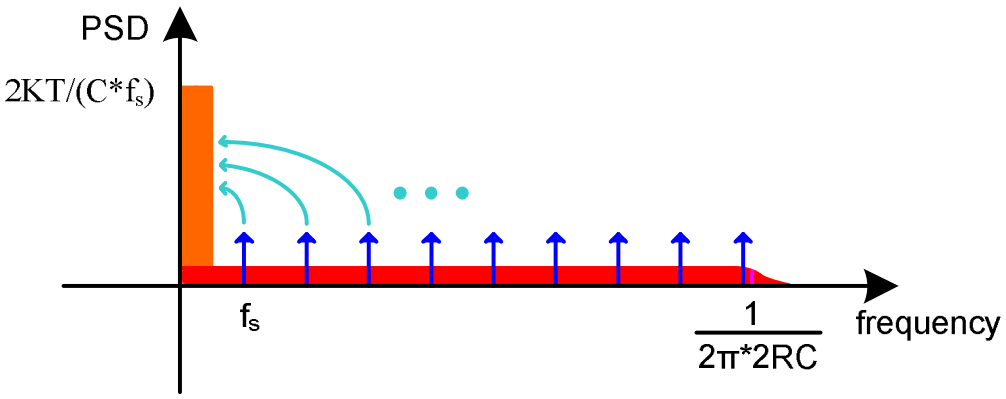


Figure 3.14: Noise folding during the sampling phase

During the integration phase, the situation is slightly more complex since the circuit has a DC supply, implying thermal unequilibrium. From the knowledge of thermal dynamics, any capacitor (C) at thermal equilibrium has an average energy of KT/2, which translates to $\overline{V_c^2}$ = KT/C. In case of thermal unequilibrium, the noise voltage on the capacitor can be derived in terms of both $V_{n,r}$ and $V_{n,o}$, and the derivation is shown in Eq. 3.26 assuming infinite R_{out}. The in-band noise power on the capacitor ($\overline{V_{c,2}^2}$) during the integration phase is shown in Eq. 3.27, considering the oversampling effect. The constant λ depends on the amplifier topology and the specific fabrication process, and it is usually 2-5 for short-channel devices.

$$\begin{aligned} &\left(V_{n,r} - i\cdot 2R - V_{c2} - V_{n,o}\right)\cdot g_m = i = V_{c2}\cdot SC_s \\ &\Rightarrow V_{c2} = \frac{V_{n,r} - V_{n,o}}{1 + SC_s\left(\frac{1}{g_m} + 2R\right)} \end{aligned} \tag{3.26}$$

$$\begin{aligned} \overline{V_{c,2}^2} &= \left(4KT\cdot 2R + 4KT\cdot\frac{\lambda}{g_m}\right)\cdot\frac{\pi}{2}\cdot\frac{1}{2\pi\cdot 2RC_s\left(1+\frac{1}{2R\cdot g_m}\right)}\cdot\frac{1}{OSR} \\ \Rightarrow \overline{V_{c,2}^2} &= \boxed{\frac{KT}{C_s\cdot OSR}\cdot\frac{\lambda + 2R\cdot g_m}{1+2R\cdot g_m}} \end{aligned} \tag{3.27}$$

In Eq. 3.28, the quantities $\overline{V_{c,1}^2}$ and $\overline{V_{c,2}^2}$ are summed to find the total input-referred in-band thermal noise power. It turns out that the in-band thermal noise of the SC integrator can be roughly modeled with a capacitor $C_s/2$ at thermal equilibrium. Fig. 3.15 shows the output spectrums of a SC delta-sigma modulator with the KT/C noise (red) and without the KT/C noise (blue). It is clearly seen that the in-band noise

floor is dominated by the KT/C noise and the high frequency spectrum is dominated by the quantization noise. For an OSR of 128, a 0.2 pF capacitor produces an in-band noise voltage of 40 μV, which gives a maximum SNR of 82 dB for a 1.5 V reference voltage. To achieve better resolution, the sampling capacitor can be increased accordingly, but this would also affect the power consumption of the system, clock frequency, and silicon overhead. Thus, the choice of C_s is a tradeoff.

$$\overline{V_c^2} = \overline{V_{c,1}^2} + \overline{V_{c,2}^2} = \boxed{\frac{2KT}{C_s \cdot OSR} \cdot \left(1 + \frac{1}{2} \cdot \frac{\lambda - 1}{1 + 2R \cdot g_m}\right)} \tag{3.28}$$

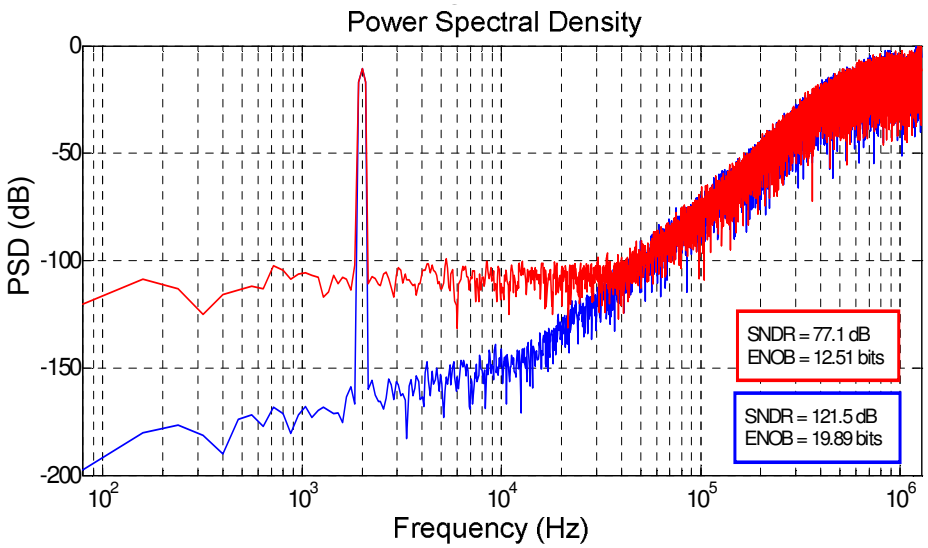


Figure 3.15: KT/C noise versus quantization noise

2. Clock jitter

Another major noise source is clock jitter. Clock jitter refers to the temporal variation of the clock period at a given point, which is measured on a cycle-to-cycle basis and can be modeled as a random variable. On the contrary, clock skew refers to the spatial variation in the arrival time of a clock transition, which is a static quantity [Rabaey02]. Table 3.1 compares clock jitter and clock skew in terms of characteristics, impacts, and sources. In digital circuits, both jitter and skew affects the maximum frequency of operation; in analog circuits, such as the SC integrator, jitter is a more important measure since it limits the sampling accuracy of the clock signal.

Table 3.1: Clock jitter versus clock skew

	Characteristics	Impacts	Sources
Jitter	Temporal variation, Dynamic quantity, Random error	Always degrade the clocking accuracy	Clock-signal generation, Power supply variation, Capacitive coupling
Skew	Spatial variation, Static quantity, Systematic error	Depends on the direction of skew: positive or negative	Device mismatch, Interconnect mismatch, Temperature variation

Fig. 3.16 shows the sampling diagram consisting of a sinusoidal input signal and a jittery clock. According to the central limit theorem, clock jitter is a summation of many small random variables, thus it has a probability density function (PDF) of

Gaussian distribution with zero mean value. The quantity Δt is the standard deviation (σ) of the Gaussian PDF. When the sampling clock is jittery, the actual sampled voltage differs from the ideal voltage at the nominal sampling instant, and the voltage difference ΔV is determined by the slope of the signal waveform and the time deviation Δt. Since a sinusoidal waveform has maximum slope at the zero-crossings, the maximum slope can be used to predict the worst-case jitter-induced noise voltage.

Eq. 3.29 and 3.30 shows the derivation of ΔV and the maximum SNR of the oversampling ADC considering only jitter noise, respectively. The SNR_{max} is determined by the ratio of the signal period T_{sig} and the clock jitter Δt. Since the sampling happens before the integration, the jitter noise will not be high-pass filtered by the modulator. In reality, the jitter-induced SNR_{max} should be kept at least 10 dB higher than the target SNR performance of the ADC, and the input KT/C noise still dominates.

$$\Delta V = \Delta t \cdot \frac{\partial\left[\frac{V_{ref}}{2}\sin\left(\omega_{sig}t\right)\right]}{\partial t} = \frac{\Delta t \cdot \pi \cdot V_{ref}}{T_{sig}} \tag{3.29}$$

$$\begin{aligned} SNR_{\max} &= 20\log_{10}\left(\frac{V_{sig}}{V_{noise}}\right) = 20\log_{10}\frac{V_{ref}\Big/\left(2\sqrt{2}\right)}{\Delta V\Big/\sqrt{OSR}} \\ &\approx \boxed{-19 + 20\log_{10}\left(\frac{T_{sig}}{\Delta t}\sqrt{OSR}\right)} \end{aligned} \tag{3.30}$$

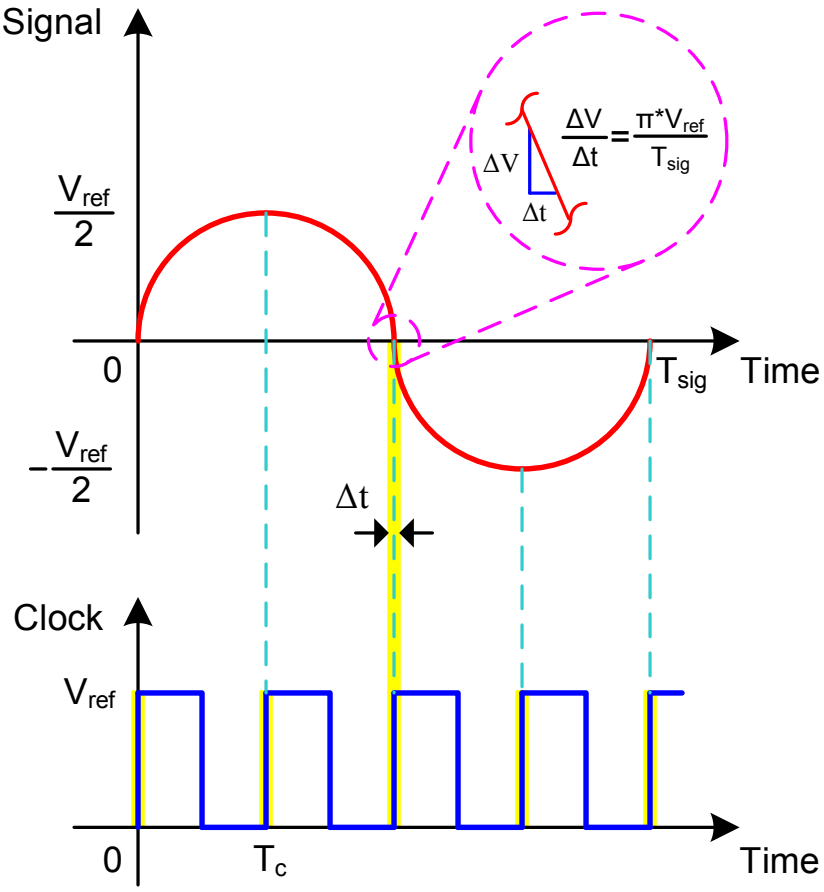


Figure 3.16: Sampling diagram with clock jitter

C. Distortion Sources

Aside from the random noise sources, nonlinear response of SC circuits would produce harmonic distortions in the output spectrum, and this deterministic error degrades the SNDR performance of the modulator especially for large input signals. Depending on specific applications, such as an audio codec, the harmonic distortion may be a more serious concern than the random noises.

As discussed in previous sections, amplifier gain nonlinearity and slew-rate limiting effect are the major factors for the harmonic distortion in SC circuits. In this section, additional distortion sources will be analyzed at both the system and circuit levels and their specific contributions to the nonlinear tones will be identified.

1. Mismatch in the differential paths

The symmetry of fully differential amplifiers tends to cancel out the even-order harmonic terms in the transfer function. Eq. 3.31 gives the transfer function of a single-ended amplifier in the Volterra series, from which the transfer function of a differential amplifier can be derived, as shown in Eq. 3.32. It is noted that the even-order harmonics are eliminated since they have the same amplitude and polarity at both the positive and negative outputs. For a sinusoidal input (ω_{sig}), the output spectrum contains both the fundamental tone (ω_{sig}) and odd-order harmonic tones ($3\omega_{sig}$, $5\omega_{sig}$, and $7\omega_{sig}$ …) decreasing in amplitude, and ideally no even-order harmonic tones ($2\omega_{sig}$, $4\omega_{sig}$, and $6\omega_{sig}$ …) would show up. This holds true for other fully-differential circuits as well, such as SC circuits.

$$y_{se}(x) = a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4 + a_5 x^5 + \cdots \tag{3.31}$$

$$y_{diff}(x) = y\left(\frac{x}{2}\right) - y\left(-\frac{x}{2}\right) = a_1 x + a_3 \frac{(x)^3}{4} + a_5 \frac{(x)^5}{16} + \cdots \tag{3.32}$$

Due to fabrication resolution, DC offset, and voltage dependence of the components, however, there are no ideally fully-differential circuits in reality. In a standard 0.13 μm CMOS process, a 100 μm by 100 μm MIM capacitor has an absolute error of 0.5% and a mismatch error of 0.05%. For smaller on-chip capacitors, the errors would be bigger. In addition, the use of on-chip resistor is usually avoided in the signal path since its value is even more loosely controlled.

Considering these mismatch effects in the differential paths, the actual transfer function of a differential amplifier would contain finite even-order harmonic tones, as shown in Eq. 3.33, where Δa_2 and Δa_4 model the difference in the even-order coefficients a_2 and a_4.

$$y_{diff}(x) = a_1 x + \Delta a_2 \frac{(x)^2}{2} + a_3 \frac{(x)^3}{4} + \Delta a_4 \frac{(x)^4}{8} + a_5 \frac{(x)^5}{16} + \cdots \tag{3.33}$$

2. Even-order harmonic distortion

In the previous section, the generation of Δa_2 and Δa_4 terms is explained and related to the differential path mismatch. However, that is only the necessary condition for the even-order harmonic distortion, not the sufficient one. This section discusses the actual generation of the even-order coefficients a_2 and a_4.

Intuitively, the even-order harmonic terms results from the signal-dependence of electrical components or the voltage references along the signal path. One of the major contributory factors is the nonlinearity of sampling capacitors. Due to the voltage-induced polarization of dielectric, on-chip capacitors have non-zero voltage-coefficient depending on the structure. In some circuits such as the VCO, a variable capacitor (Varactor) is needed to tune the oscillation frequency, and the voltage-dependence is desired. In many other cases, such as the SC circuits, the voltage dependence causes the undesired even-order harmonic terms. Eq. 3.34 shows the simplified model of a nonlinear capacitor, and Eq. 3.35 shows the resulting transfer function of a SC amplifier based on the nonlinear capacitor, assuming all the other factors ideal. Clearly, there is a 2^{nd}-order term in the transfer function.

$$C_s(V) = C_0 + C_1 V \tag{3.34}$$

$$y(x) = \frac{x \cdot C_s(x)}{C_f} = \frac{C_0}{C_f} x + \frac{C_1}{C_f} x^2 \tag{3.35}$$

Another major distortion source belongs to the signal-dependent feedback voltages, though it is more subtle. In a single-bit quantizer, for example, the two voltage levels are related to the power supplies. The power supplies might slightly rise or fall as the modulator draws more or less current from the supply for different input amplitudes, therefore the two output levels somehow become a function of the input signals that they are being used to represent. In addition, this supply variation may also cause the charge injection of MOS switches signal-dependent as well, since the clock signals are also derived from the power supplies. Therefore, it is important

to have well-regulated power supplies on both the quantizer and buffers for the clock signals.

3. Nonideal switches

It is worthwhile to investigate the limitations of MOS switches more carefully. Fig. 3.17 shows the input sampling circuit and the associated timing diagram. In the sampling phase, the MOS switches M_{1n} and M_{1p} are operating in the linear mode, and the channel charges can be given by Eq. 3.36 and 3.37. The total channel charges of the input switches can be calculated as shown in Eq. 3.38, assuming M_{1n} and M_{1p} have the same size. When the input switches are closed, the channel charges go in two directions: the signal source (harmless) and the sampling capacitor. The divide ratio is a complex function of the instantaneous input voltage [Wegmann87]. In addition, the threshold voltages V_{tn} and $|V_{tp}|$ are also a nonlinear function of the input voltage, due to the body effect. Therefore, the nonlinearity in the circuit is also related to the signal-dependent charge injection from the input switches.

$$Q_{1n} = -C_{ox}\left(WL\right)_{1n}\left(V_{dd} - V_{in} - V_{tn}\right) \tag{3.36}$$

$$Q_{1p} = C_{ox}\left(WL\right)_{1p}\left(V_{in} - \left|V_{tp}\right|\right) \tag{3.37}$$

$$Q_{1} = C_{ox}\left(WL\right)_{1}\left(2V_{in} + V_{tn} - \left|V_{tp}\right| - V_{dd}\right) \tag{3.38}$$

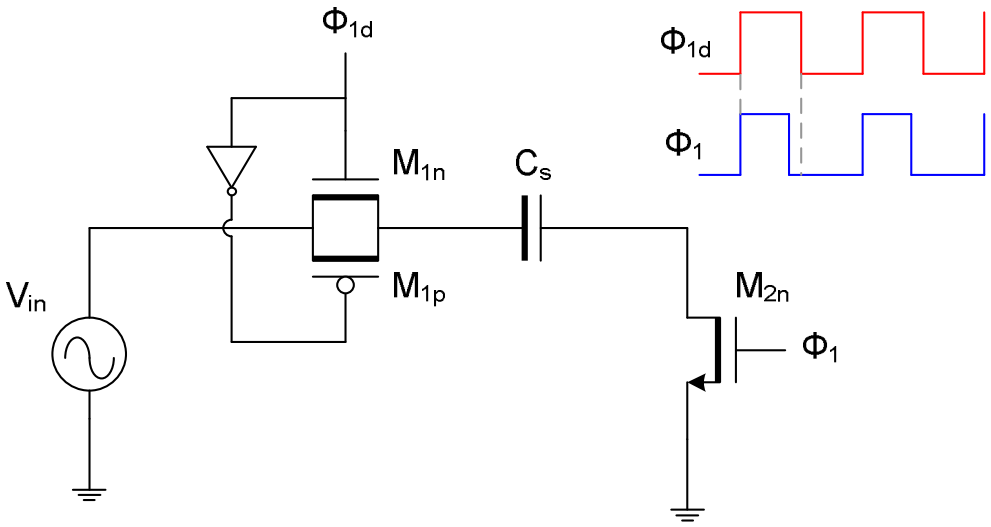


Figure 3.17: Input sampling circuitry of SC circuits

To mitigate this problem, the bottom-plate sampling technique can be utilized: the switch M_{2n} is turned off slightly earlier than the switch M_1. By turning M_{2n} off earlier, the capacitor C_s becomes a high-impedance node and all of Q_1 would go to the signal source. Since the terminal voltages of M_{2n} are fixed in the steady-state, its charge injection only causes a constant offset and can be calibrated out. In reality, the charge injection from M_{2n} also depends on the channel conductance of M_1, which is also a nonlinear function of the input signal. Thus, the switch M_{2n} may also contribute to the output harmonic distortion in the SC circuit.

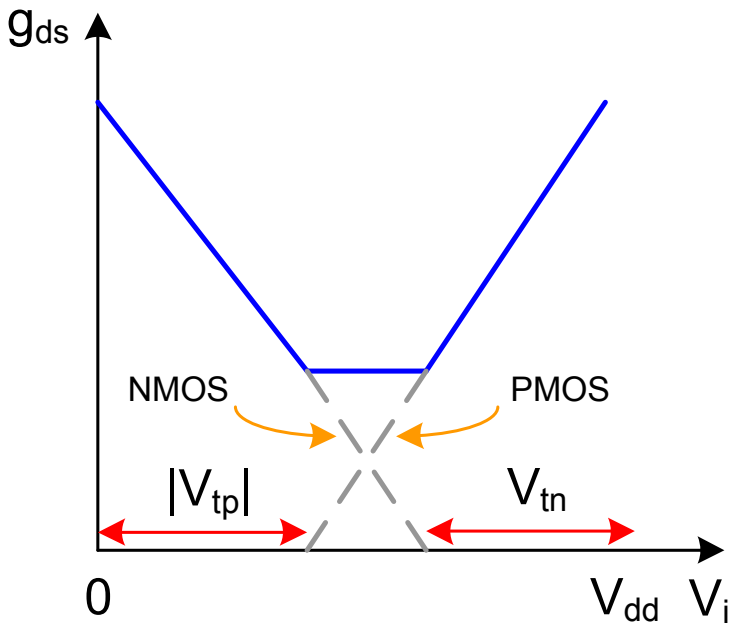


Figure 3.18: Conductance of a transmission gate switch

Fig. 3.18 shows the voltage dependence of the channel conductance of MOS switches, formed by a CMOS transmission gate [Abo99]. The channel conductance determines the time constant of the input sampling circuit, which becomes a function of voltage. If the bandwidth of the input circuit is low, the signal-dependent time constant would give rise to large distortion, and this distortion also increases with the signal frequency. It is therefore important to have sufficiently large switch conductance to avoid this problem.

IV. SYSTEM CONSIDERATIONS

After elaborating the relevant circuit nonlinearities in the ADC design, the system architectures will be discussed in this chapter in different aspects, pertaining to the micro power delta-sigma modulator design in the dissertation.

A. Delta-Sigma versus Nyquist-Rate

Basically, the delta-sigma ADC is unique in that it is a feedback system, while most nyquist-rate ADCs have an open-loop structure. Due to the use of feedback, the delta-sigma ADC has an advantage that coarse analog blocks can be utilized to form the loop. Hence, there is more flexibility in optimizing the power efficiency, resolution, and silicon overhead in the delta-sigma ADC design. On the contrary, the open-loop structure in nyquist-rate ADCs implies that the circuit nonidealities directly translate into the achievable resolution of the ADC. Therefore, it is more important to have high-performance analog blocks in the nyquist-rate ADC design, and in many cases digital calibration circuitry needs to be exploited as well to mitigate the component mismatching, which inevitably increases the power consumption and silicon overhead for the ADC.

Fig. 4.1 shows a "zodiac" of ADC architectures in terms of bandwidth and resolution, redrawn from [Silva04]. Due to the oversampling requirement, the delta-sigma ADC is mostly used for low frequency and high resolution applications. It is noted that the SAR ADC may also be a feasible solution for the neural implant applications [Harrison07]. Table 4.1 compares the pros and cons of the delta-sigma

ADC with the SAR ADC. The relaxed requirements on the analog blocks of the delta-sigma ADC make it possible to trade the resolution for higher power efficiency. In addition, the decimation filter may be implemented in an off-chip PC board. Hence, it is the choice of the ADC architecture in the HDNI.

Table 4.1: Delta-sigma ADC versus SAR ADC

	SAR	Delta-Sigma
Pros	Easy multiplexing; Better control on the sampling point	High resolution; small form factor; Coarse analog blocks can be used
Cons	Calibration circuitry needed; Complex anti-aliasing filter needed	Long conversion latency; Decimation filter needed

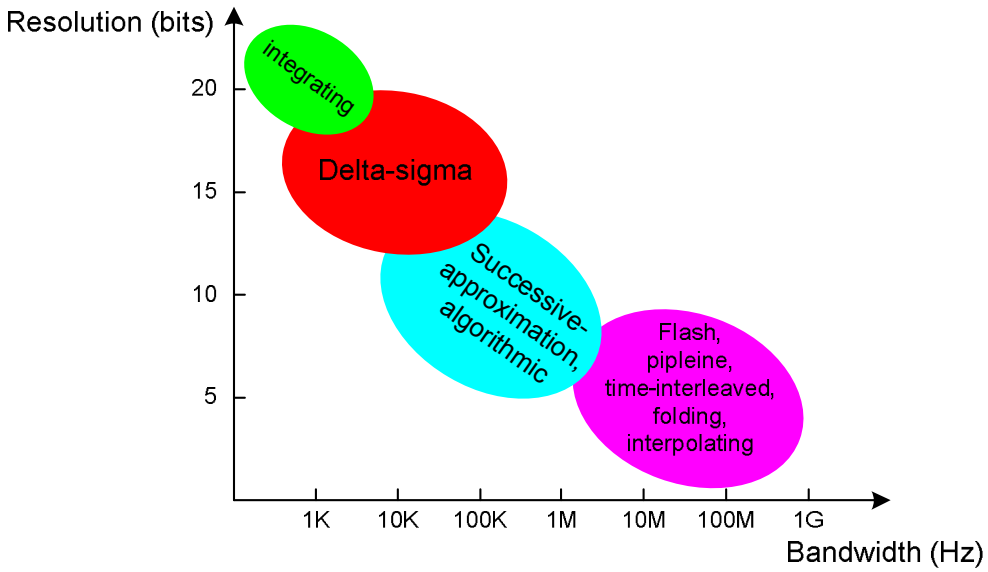


Figure 4.1: Zodiac of ADC architectures

B. Discrete-Time versus Continuous-Time

The above discussion of the delta-sigma ADC is based on the discrete-time structure, implemented with switched-capacitor circuits. In many high-frequency applications, the continuous-time (CT) delta-sigma ADC, implemented with active-RC or Gm-C filters, is often seen and demonstrates unique advantages.

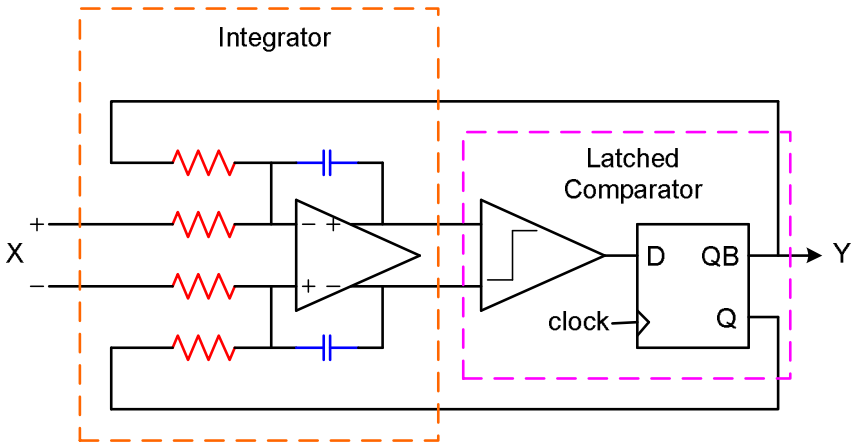


Figure 4.2: Circuit diagram of the continuous-time delta-sigma modulator

Fig. 4.2 shows the active-RC implementation of the first order delta-sigma modulator. Since switches are eliminated, the CT delta-sigma modulator is better suited for low-voltage design, which implies lower power consumption. Even though bootstrapped switches can be used in the DT implementation [Abo99], the circuit complexity is greatly increased and the switches may break down during long-term operation. Both the CT and DT implementations are possible only in CMOS processes if the decimation filter will be included on the same die.

Furthermore, there is no settling requirement for the amplifier in the CT implementation. Therefore, it can be operated at higher clock frequency for the same

power dissipation. In fact, over 20MHz CT delta-sigma modulator has been reported [Park09]. For the DT implementation, the clock period needs to be 5-10 times larger than the time constant of the SC integrator for achieving sufficient settling accuracy in MASH architectures.

Since the sampling action happens after the loop filter in the CT implementation, the KT/C noise, which haunts the DT modulator, is not a concern for the CT modulator [Li06]. In addition, this also realizes an inherent anti-aliasing filter (AAF), reducing the overall system complexity. For a wide-bandwidth DT delta-sigma ADC design, the AAF design may become an issue.

On the other hand, the loop coefficients of the DT implementation are determined by capacitor ratio, while the loop coefficients of the CT implementation depend on the absolute values of the loosely controlled on-chip resistors. Therefore, additional tuning circuitry needs to be added in the CT modulator to adjust the loop coefficient on the fly. This extra complexity prevents its use in the MASH architecture, while the DT MASH modulator can be easily implemented to attain better tradeoff between resolution, signal bandwidth, and power efficiency.

Moreover, the loop coefficients of the DT implementation are independent of the clock frequency. That means the resolution of the DT modulator is scalable by adjusting the clock frequency, hence it can be easily reused for different signal bandwidth and applications. On the contrary, the loop coefficients of the CT implementation are related with the clock frequency, so the CT modulator is mainly designed at a fixed clock frequency. Due to the same reason, the CT modulator is

more sensitive to clock jitter than the DT modulator, and this potentially limits the frequency of operation in the CT modulator.

Table 4.2 compares the DT and CT modulators. Although the CT modulator may be more suited for lower power consumption and higher frequency of operation, the DT modulator is preferred in terms of system efficiency, design flexibility and process robustness.

Table 4.2: CT modulator versus DT modulator

	DT modulators	CT modulators
Low voltage operation	Difficult	Easier
Power consumption	More	Less
Signal bandwidth	Low-medium	Medium-high
Clock jitter sensitivity	Low	High
Anti-aliasing filter	Required	Inherent available
Process robustness	High	Low
Tuning circuitry	Usually not required	Required
Loop filter scalability	Yes	No
MASH architecture	Easy	Difficult

C. Single-Loop versus MASH

To achieve more resolution, a higher order delta-sigma modulator can be utilized. As the order of the modulator increases, however, the feedback system may become unstable and the modulator output generates a long sequence of "one" or "zero" [Candy85]. In this section, some linear approximation is made to gain an intuitive understanding of the stability problem.

Since the sampling delay effect of the SC integrator can be neglected due to oversampling, an S-domain method can be applied and each integrator is treated as a high-gain amplifier with -90º phase delay. For the first order modulator, the phase margin (PM) of the loop is 90º, thus it will be unconditionally stable for any input within the full-scale range. For the second order modulator, the PM of the outer feedback loop becomes 0º since there are two integrators in the signal path. Although the inner compensation loop has a 90º PM, the modulator becomes conditionally stable depending on the input amplitude [Schreier04]. For large input amplitudes, the output voltages of the integrators may approach the rails, greatly saturating the amplifier gain. In that case, the feedback loop becomes weak in bringing the modulator back into normal operation, and the modulator would generate more in-band noise and harmonic distortion. For a higher-order modulator, the stability condition is more severe and the loop filter needs to be more carefully balanced. In fact, the loop stability of the delta-sigma modulator depends on many factors such as total quantization noise power, the effective quantizer gain, and the out-of-band magnitude of the NTF [Lee90].

In order to achieve high resolution and stable operation, lower order modulators can be cascaded in a multi-stage manner, as shown in Fig. 3.4. In the 2-2 MASH modulator, the quantization noise of the first modulator is extracted and fed into the second modulator, but there is no recursive signal path from the lower stage to the upper stage. Therefore, a higher order noise filtering can be realized while the stability margin of the whole system is still of the lower order. Table 4.3 summarizes the pros and cons of the single-loop delta-sigma modulator and MASH modulator.

Table 4.3: Single-loop versus MASH

	Single-loop modulator	MASH
Pros	Insensitive to the analog blocks; Insensitive to gain mismatch; Less out-of-band noise	More stable; Higher dynamic range; More design flexibility
Cons	Less stable; Loop filter needs to be carefully balanced	High performance amplifier needed; Sensitive to gain mismatch; More out-of-band noise

D. Single-Bit versus Multi-Bit

In many delta-sigma modulator implementations, a single-bit quantizer is utilized for its perfect linearity. A single-bit modulator requires no digital correction logic for the feedback DAC nonlinearity, realizing less silicon overhead and design complexity. In a high resolution modulator design, a multi-bit quantizer may be used to lower the total quantization noise power [Yu05]. Due to the feedback, however, the nonlinearity of the multi-bit DAC directly affects the accuracy of the ADC. Thus, digital correction logic needs to be employed in a multi-bit modulator to calibrate out the DAC nonlinearity. Table 4.4 compares the pros and cons of these two quantizer configurations in the DT delta-sigma modulator design.

Table 4.4: Single-bit modulator versus multi-bit modulator

	Single-bit	Multi-bit
Pros	Inherent linearity; Simple design; Less silicon overhead; Less power consumption	Lower quantization noise; Lower slew rate requirement; Higher dynamic range; More stability margin
Cons	More quantization noise; More slew rate requirement; Lower dynamic range; Less stability margin	Digital correction logic required; More design complexity; More silicon overhead; More power consumption

E. Opamp versus Inverter Amplifier

Conventional Opamp, based on differential amplifier, is usually utilized to form the loop filter in the design of delta-sigma modulators. Due to the current-biasing, Opamp achieves a wide input common-mode range, and the transistor sizing is also relatively straightforward. On the other hand, Opamp will be subject to the slew-rate limiting effect under large input excitations, affecting not only the settling accuracy but also harmonic distortion.

To address this problem, an inverter amplifier, employing voltage-biasing, can be utilized and demonstrates unique advantages. Traditionally, inverter is used in digital circuits to provide logic transition and the transition slope is not important. In analog circuits, however, an inverter can be biased in the transition region for amplification. These two amplifier topologies will be compared in this section.

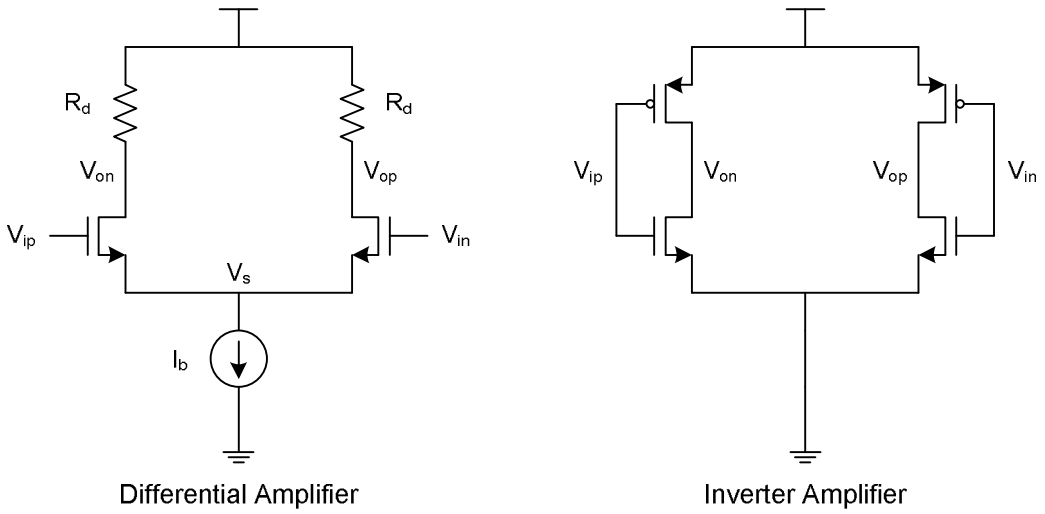


Figure 4.3: Current-biased Opamp versus voltage-biased inverter amplifier

Fig. 4.3 shows a simplified comparison between the current-biased differential amplifier and the voltage-biased inverter amplifier. In the differential amplifier, an externally-referred current source is used to setup the DC operating point for the amplifier, and the input CM voltage would not directly affect the static current. Under large input excitations, the constant current I_b will limit the maximally-achievable rate of change of the output voltage. On the contrary, the DC operating point in the inverter amplifier is set by the input/output CM voltages, and therefore the dynamic current I_d during the output slewing can be much larger than the static current I_s. Fig. 4.4 shows the step response of the inverter amplifier in a negative feedback. The slew-rate limiting effect is greatly mitigated. Hence, the inverter amplifier can be biased at very low static current through proper transistor sizing, while still achieving reasonable speed of operation.

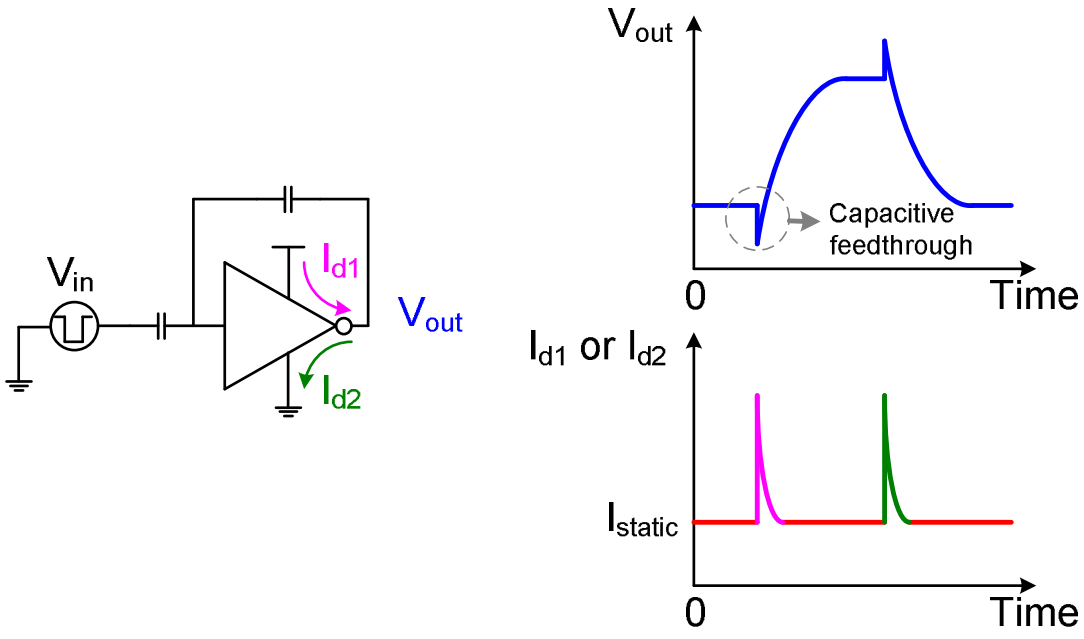


Figure 4.4: Current and voltage responses of an inverter amplifier

In the differential amplifier, the AC ground at the common-source node V_s realizes a relatively high DM gain while suppressing the CM gain. However, this greatly relies on the output resistance of the current source. In addition, the differential amplifier is also not perfectly symmetrical in reality due to manufacturing variations. Thus, the CM input may contribute to the DM output and vice versa as shown in Eq. 4.1 and 4.2, affecting signal integrity [Gray04]. A cascode current source can be utilized to mitigate this nonideality. In scaled CMOS processes, however, this may become very challenging due to the reduction of voltage headroom and short-channel effects.

$$A_{cm-dm} = \left.\frac{V_{od}}{V_{ic}}\right|_{V_{id}=0} = -\frac{g_m \cdot \Delta R + \Delta g_m \cdot R}{1 + 2 g_m r_{tail}} \tag{4.1}$$

$$A_{dm-cm} = \left.\frac{V_{oc}}{V_{id}}\right|_{V_{ic}=0} = -\frac{1}{4}\left(g_m \cdot \Delta R + \frac{\Delta g_m \cdot R}{1 + 2 g_m r_{tail}} \right) \tag{4.2}$$

In contrast, the inverter amplifier is an over-driven device since no voltage headroom is taken up by the current source. This means threshold voltage variation in the inverter amplifier produces less transconductance variance Δg_m. Furthermore, the switching threshold V_M of inverter, defined as the point where $V_{in} = V_{out}$, is also relatively insensitive to variations in the device ratio. Eq. 4.3 gives the expression for the V_M of inverter, assuming short-channel devices used. In addition, inverter is usually sized to balance the driving strengths of the transistors for maximum noise margins and symmetrical DC characteristics. Eq. 4.4 shows the required ratio of PMOS versus NMOS transistor sizes to achieve a desired V_M. Generally speaking,

V_M is relatively insensitive to variations in the device ratio, and small variations of the ratio do not disturb the transfer characteristic very much [Rabaey02]. Therefore, it is generally an advantage to use inverter amplifiers in the SC circuit for a mismatch-tolerant design. Table 4.5 summarized the key differences between conventional Opamp and inverter amplifier. In the next chapter, several novel self-biased inverter amplifiers will be presented, which employ internal negative feedback to attain better performance.

$$V_M = \frac{\upsilon_{satn} W_n \left(V_{Tn} + \frac{V_{DSATn}}{2} \right) + \upsilon_{satp} W_p \left(V_{dd} - \left| V_{Tp} \right| - \frac{V_{DSATp}}{2} \right)}{\upsilon_{satp} W_p + \upsilon_{satn} W_n} \tag{4.3}$$

$$\frac{W_p}{W_n} = \frac{\upsilon_{satn} W_n \left(V_M - V_{Tn} - V_{DSATn}/2 \right)}{\upsilon_{satp} W_p \left(V_{dd} - V_M - \left| V_{Tp} \right| - V_{DSATp}/2 \right)} \tag{4.4}$$

Table 4.5: Opamp versus Inverter amplifier

	Opamp	Inverter amplifier
Pros	High DM gain Good CM rejection Variable input CM voltage	High dynamic current Better power efficiency Variation tolerance possible
Cons	Relies on the current source Variation sensitive Slew-rate limited	Need to improve DM gain Need to improve CM rejection Fixed input CM voltage

V. CIRCUIT INNOVATIONS

In this chapter, the circuit-level innovations of the dissertation are presented: a suite of self-biased inverter amplifier and floating CDS circuit. These inverter amplifier topologies were created by Prof. Theogarajan for achieving high power and area efficiency in the ADC design. To apply the inverter amplifier in MASH architectures, the floating CDS circuit is devised to improve the amplifier gain linearity and enhance the matching accuracy of loop filter.

A. The Super Inverter

Fig. 5.1 shows the circuit diagram of the self-biased super inverter amplifier. Compared to a pair of CMOS inverters, the super inverter adds the cross-coupled cascode stage for differential-mode gain boosting, and the complementary source degeneration stages for common-mode noise rejection and optimum self-biasing. The key idea behind this amplifier is that it responds differently to the differential-mode and common-mode signals, and does not rely on the output resistance of a current source to achieve high common-mode noise rejection (CMRR) or power supply noise rejection (PSRR). In addition, the internal negative feedback loop provides a way to stabilize the DC operating point, and any shift in the nominal bias voltages due to variations in process parameters or operating conditions is corrected through the negative feedback [Bazes01].

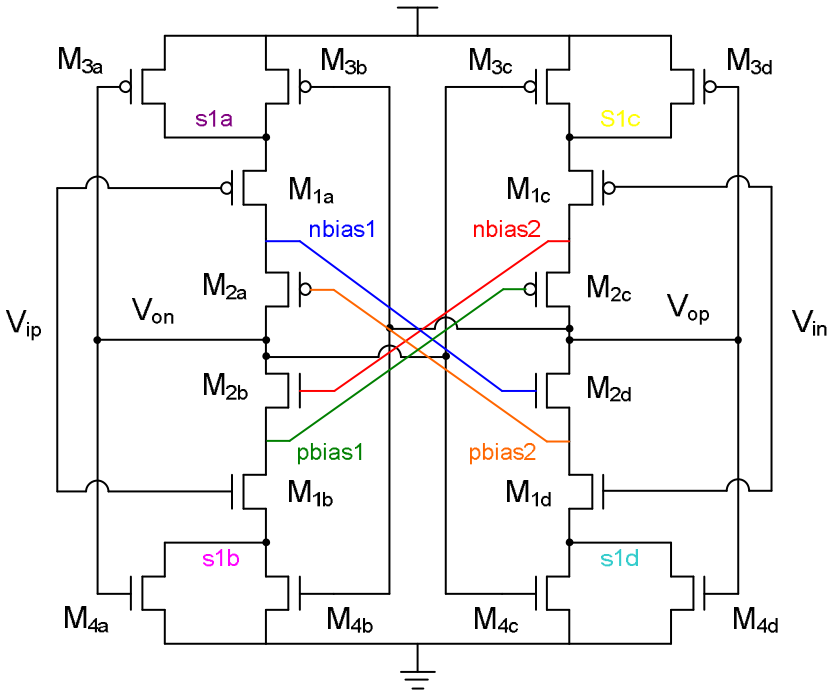


Figure 5.1: Circuit diagram of the super inverter

1. Operation principles

As shown in Fig. 5.1, M_1 serves as the push-pull differential input stages. $M_{3,4}$ form a complementary source degeneration for M_1, with their gate voltages complementarily biased by the differential outputs, V_{op} and V_{on}. By biasing $M_{3,4}$ complementarily, the common-mode gain (A_{cm}) of the super inverter will be suppressed, while the differential-mode gain (A_{dm}) is largely unaffected. The A_{dm} is boosted utilizing the cross-coupled cascode stage, which only affects the DM operation. In the following, the gain derivations are conducted base on small-signal assumption. For large-signal inputs, the internal positive feedbacks will change the operation mode of the super inverter, which will be discussed.

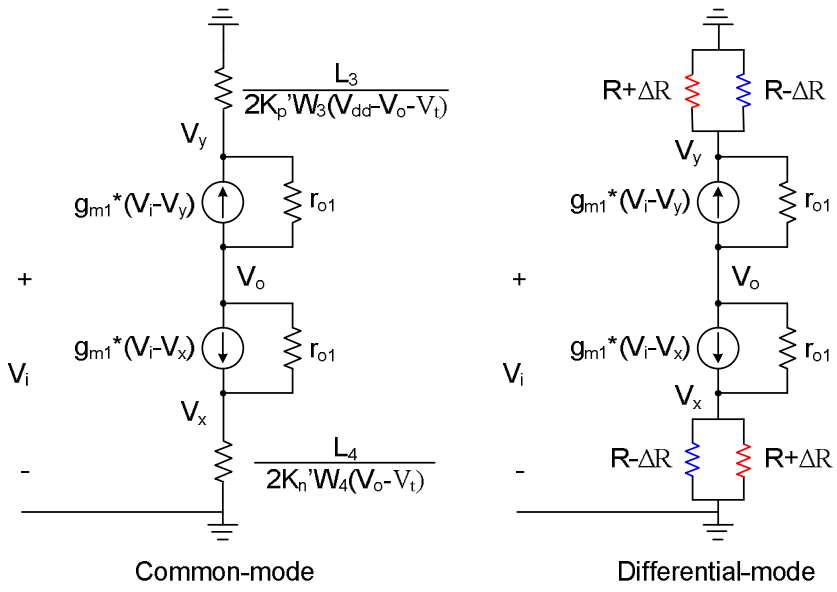


Figure 5.2: Simplified small-signal models highlighting the degeneration stages

CM gain: For the derivation of the A_{cm}, the small-signal model of the super inverter, excluding the enhanced cascode stage, is shown in Fig. 5.2. In the differential-mode operation, the biasing voltages V_{op} and V_{on} are varied differentially and the small-signal currents in the degeneration devices flow into each other. In other words, the complementary source degeneration stage can be modeled as two parallel resistors: R+ΔR and R-ΔR. Assuming ΔR/R << 1, the degeneration stage can be effectively modeled by a constant resistor: R/2. For a MOS device biased in the linear region, its output resistance is quite small, thus V_x can therefore be treated as an AC ground for the derivation of the A_{dm}. In the common-mode operation, however, the internal node voltage V_x tracks the output voltage V_o change in an opposite direction, forming a series-shunt negative feedback to suppress the A_{cm}.

Eq. 5.1-4 shows the derivation of the A_{cm}, where the I_{dc} and V_{cm} represent the nominal static current and input CM voltage, respectively. In the derivation, the cascode stage is simply neglected since it has little effect on the A_{cm}. For small-signal operations, the static current can be assumed constant due to the negative feedback of the DC path, and this assumption simplifies the small-signal analysis.

$$V_x \approx \frac{I_{dc}}{2K_n^{'}\frac{W_4}{L_4}(V_o - V_t)} \tag{5.1}$$

$$\beta = \frac{\partial V_x}{\partial V_o}\Big|_{V_o=V_{cm}} = -\frac{I_{dc}}{2k_n^{'}\frac{W_4}{L_4}(V_{cm} - V_t)^2} \tag{5.2}$$

$$I_{dc} \approx \frac{K_n^{'}}{2}\frac{W_1}{L_1}\left[V_{cm}(1+\beta) - V_t\right]^2 \tag{5.3}$$

$$A_{cm} \approx \boxed{\frac{-g_{m1}r_{o1}}{1-\beta(1+g_{m1}r_{o1})}} \tag{5.4}$$

PSRR: the power supply noise rejection (A_{supply}) shares the same signal path as the common-mode noise rejection, and therefore these two quantities should be comparable. The A_{supply} is derived by applying a test voltage at the rail, as given in Eq. 5.5. Compared to a CMOS inverter, the super inverter amplifier is much more capable in rejecting the common-mode noise and power supply noise, an important merit in high-resolution analog application.

$$A_{\sup ply} \approx \boxed{\frac{1+g_{m1}r_{o1}}{1-\beta(1+g_{m1}r_{o1})}} \tag{5.5}$$

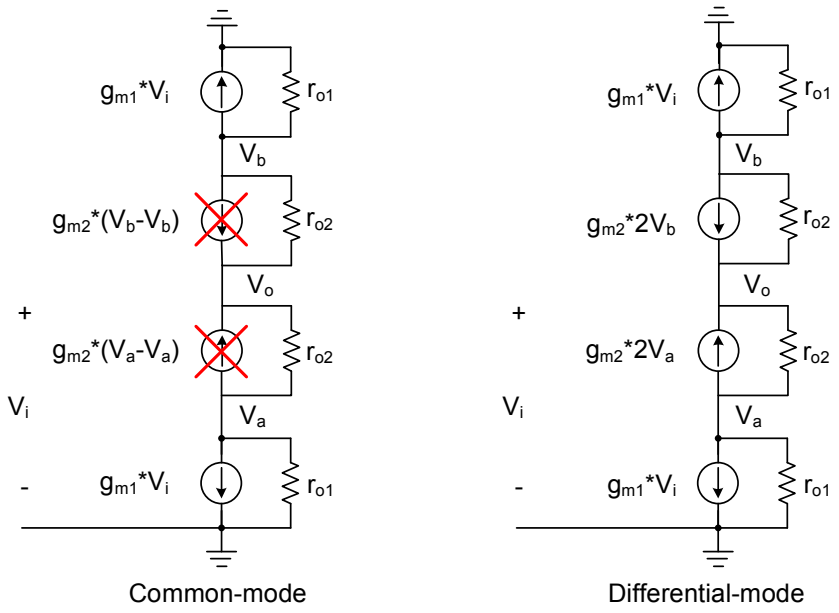


Figure 5.3: Simplified small-signal models highlighting the cascode stages

DM gain: For the derivation of the A_{dm}, the small-signal model of the super inverter, excluding the complementary source degeneration, is shown in Fig. 5.3. Cross-biased cascode stage M_2 is added to boost the A_{dm}. It operates as follows: in the differential-mode operation, the gate and source voltage of M_2 are varied in opposite directions by the differential input voltages. Assuming the driving capabilities in both the pull-up and pull-down networks match each other, these voltage changes are also differential and this doubles the effective transconductance of M_2; in the common-mode operation, the small-signal gate and source voltages of M_2 become level-shifted versions of each other, so the cascode effect mostly vanishes.

Eq. 5.6 derives the expression for the A_{dm}. In the derivation, the degeneration stage is simply neglected since its drain node is assumed as a virtual ground. In short,

the super inverter achieves high A_{dm} and low A_{cm} through the separation of the gain paths, and this is a more reliable way to realize high CMRR and PSRR.

$$A_{dm} \approx \boxed{-2 g_{m1} r_{o1} g_{m2} r_{o2}} \tag{5.5}$$

Mismatch tolerance: The super inverter is also unique in that it has an internal negative feedback loop in the circuit to stabilize the DC conditions, while the conventional Opamp basically has an open-loop structure. However, the internal positive feedback may strongly affect the tolerance performance of the amplifier. A mismatch analysis on a pair of cross-coupled inverters can be found in [Rahul91]. Due to the complexity of the super inverter, the corner simulation will be utilized instead for the variation analysis.

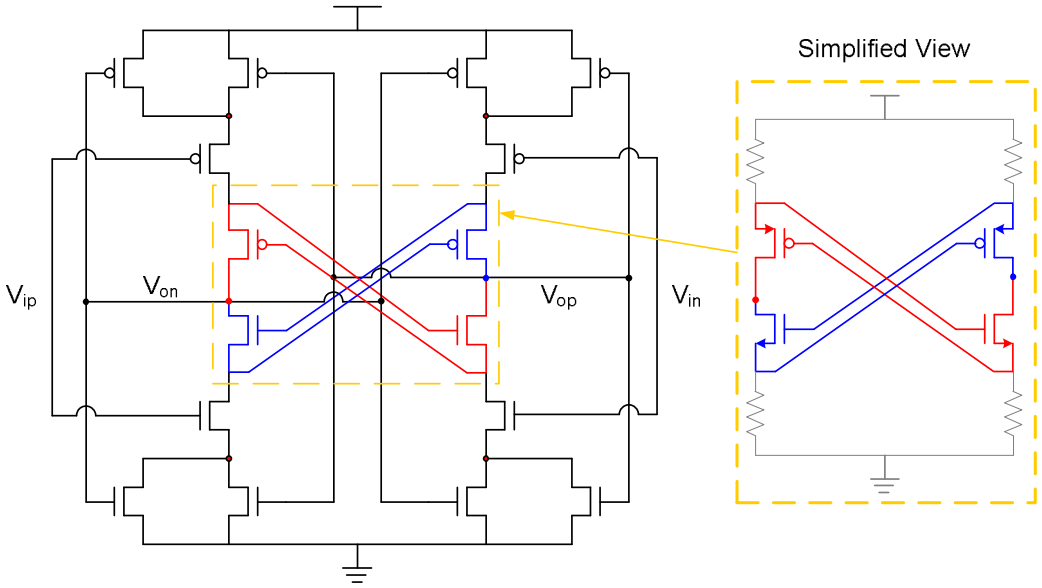


Figure 5.4: Positive feedback loops in the super inverter

Linearity: A drawback of the super inverter relates to the two positive feedback loops caused by the cross-coupled cascode stage, as illustrated in Fig. 5.4. For small-signal DM input, the input stages dominate the amplification and the positive feedback loops would not manifest themselves in the output voltage swing. For relatively large-signal DM input, the positive loop gain may become larger than one, and the output voltage of the amplifier would change radically for a small input perturbation. After the input devices (M_1) are pushed into the linear region, the amplifier gain finally saturates. In the DC transfer curve of the super inverter, three operating regions can be observed: the linear-gain region around DC, the high-gain region due to positive feedback, and the saturated-gain region. The positive feedback loops adversely affect the linearity performance of the amplifier and hence the SNDR and SFDR metrics of the ADC.

Noise: The noise performance of the super inverter is dominated by the input devices. The degeneration stage is biased in the linear region, and its noise voltage will be suppressed by the supply noise rejection path. The noise voltage of the cascode stage is degenerated by the input devices, so it also has negligible effect on the output voltage. Eq. 5.6 gives the input-referred noise density of the super inverter. Thanks to larger transconductance, the super inverter has less thermal noise than the differential amplifier at the same current density, but its low frequency 1/*f* noise will be slightly higher due to more input devices.

$$\overline{V_{n,i}^2}(f) \approx 4KT \cdot \frac{2\gamma}{g_{m1n} + g_{m1p}} + \frac{2K_n}{(WL)_{1n} C_{ox} f} + \frac{2K_p}{(WL)_{1p} C_{ox} f} \tag{5.6}$$

Sizing: The transistor sizing for the super inverter is conducted by taking advantage of its vertical and horizontal symmetries. The static current is mainly determined by the input device, so the W/L of M_1 is designed to set the desired current density. In addition, the pull-up network and pull-down network should be sized to achieve comparable driving capabilities, setting the switching threshold at the mid-rail. By matching the driving capabilities, the output range of the amplifier can also be maximized, thereby enhancing the linearity performance. The channel length of the cascode devices is made slightly larger, and this achieves 2 or 3 dB more DC gain. To make a compact layout, all the transistors are sized in such a way that they can be aligned with each other in the layout. In other words, all the PMOS/NMOS devices are made the same width and all the vertically-aligned devices should have the same length. Table 5.1 gives the transistor sizing for the super inverter at 1.5 V supply.

Table 5.1: Transistor sizing of the super inverter

	M_{1n}	M_{1p}	M_{2n}	M_{2p}	M_3	M_4
Width	0.6 µm	1.5 µm	0.6 µm	1.5 µm	1.5 µm	0.6 µm
Length	0.6 µm	0.6 µm	1 µm	1 µm	0.6 µm	0.6 µm

2. Simulation results

Fig. 5.5 shows the DC transfer curves of the super inverter. Both differential-mode and common-mode responses are simulated by sweeping the DC input voltage from 0 V to 1.5 V. Clearly, the slope of the differential-mode response at the mid-rail is much steeper than the common-mode response. In addition, the super inverter also achieves a rail-to-rail output swing, a desirable merit in some mixed-signal applications. From the DC curves, it is also noted that the super inverter has a nice gain only if its input CM voltage is biased at the mid-rail. This limitation needs to be addressed when the super inverter is employed in SC circuits.

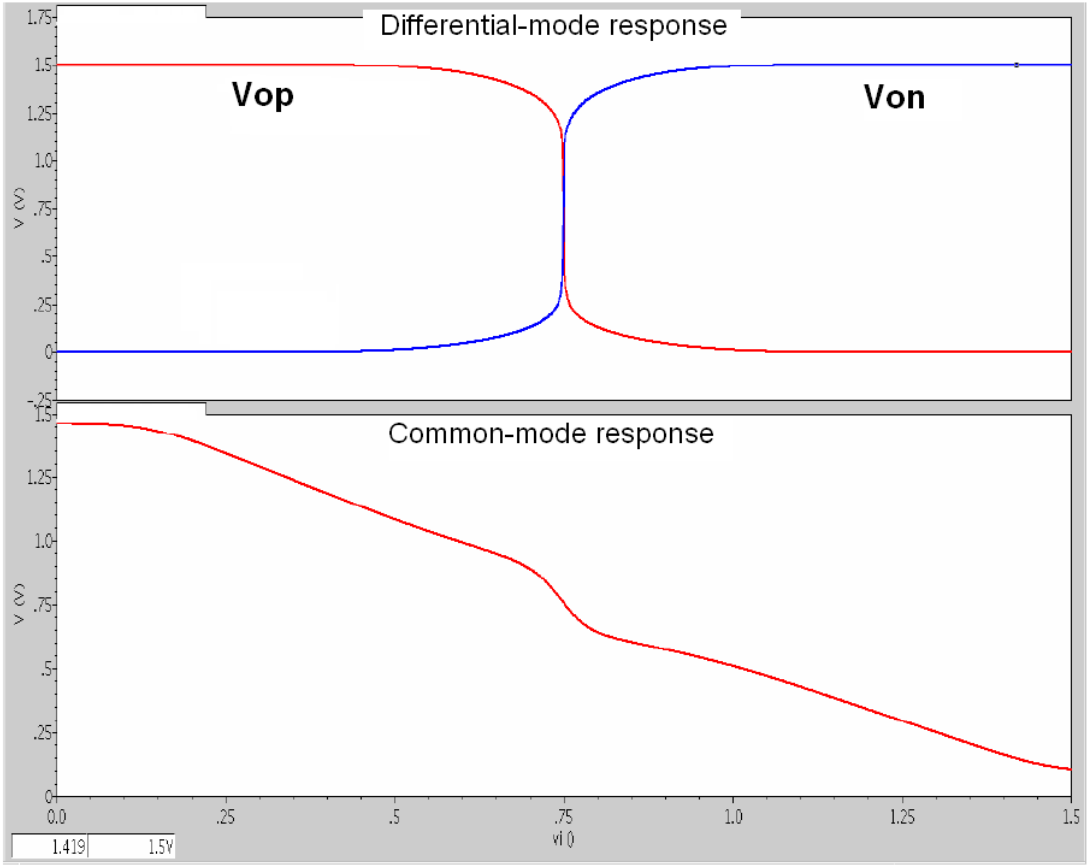


Figure 5.5: DC transfer curves of the super inverter

Fig. 5.6 shows the zoom-in view of the differential-mode DC response, with the differential input swept from -2 mV to 2 mV. Three operation regions are clearly seen in the response: linear-gain, high-gain, and low-gain. For the output swing within (0.64 V – 0.84 V), the inverter is operating in the linear-gain region. For the output swing within (0.52 V – 0.64 V) or (0.84 V – 1 V), the inverter is working in the high-gain region due to the positive feedback, and excessive harmonic distortion results. For the output swing within (0 V – 0.52 V) or (1 V – 1.5 V), the inverter enters the low-gain region, limiting the amplification accuracy. In addition, it is seen that the internal node voltages for the differential-mode operation also agree with the theoretical analysis in the previous section.

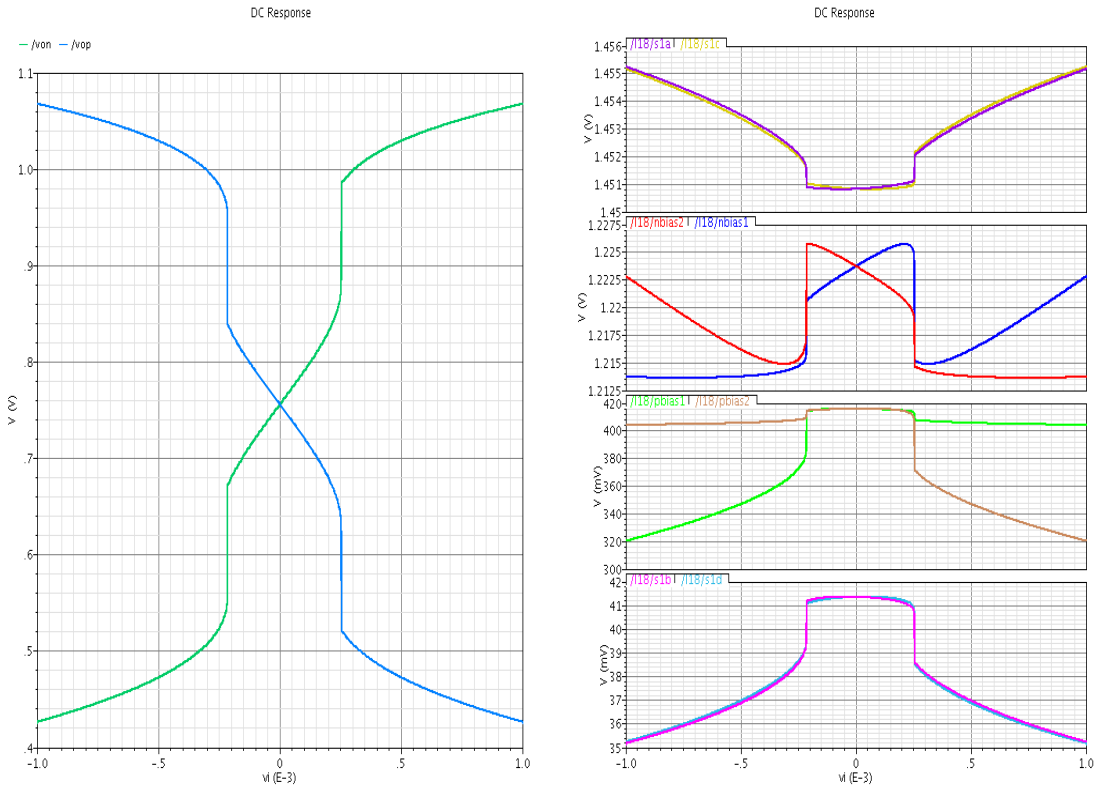


Figure 5.6: Zoom-in view of the DC response

Fig. 5.7 shows the static current drawn from the supply as the input voltage is swept. In the linear-gain region, confined by the thresholds of positive feedback, it is noted that the static current of the super inverter is relatively constant.

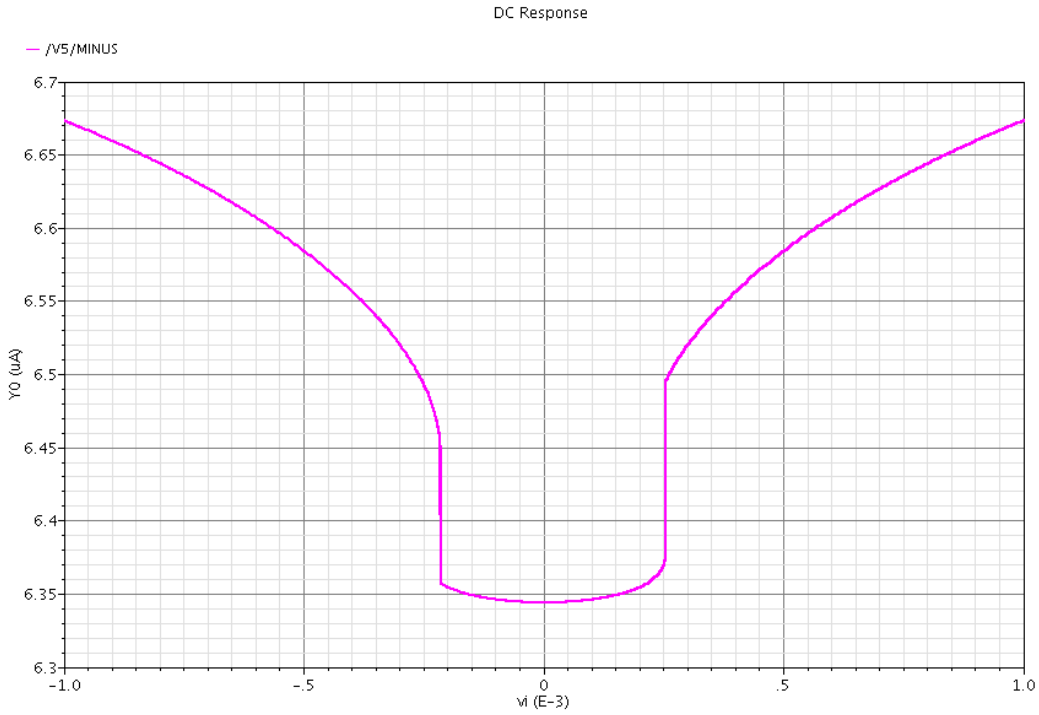


Figure 5.7: Static current of the super inverter

Fig. 5.8 shows the AC response of the super inverter loaded by an external 1 pF capacitor. From the Bode plots, the small-signal parameters, such as DC gain, bandwidth, and phase margin, can be determined. Table 5.2 summarizes the simulated characterizations of the super inverter at 1.5 V supply. In fact, both the large-signal and small-signal performances of the super inverter can be accurately predicted by the given analytical formulas.

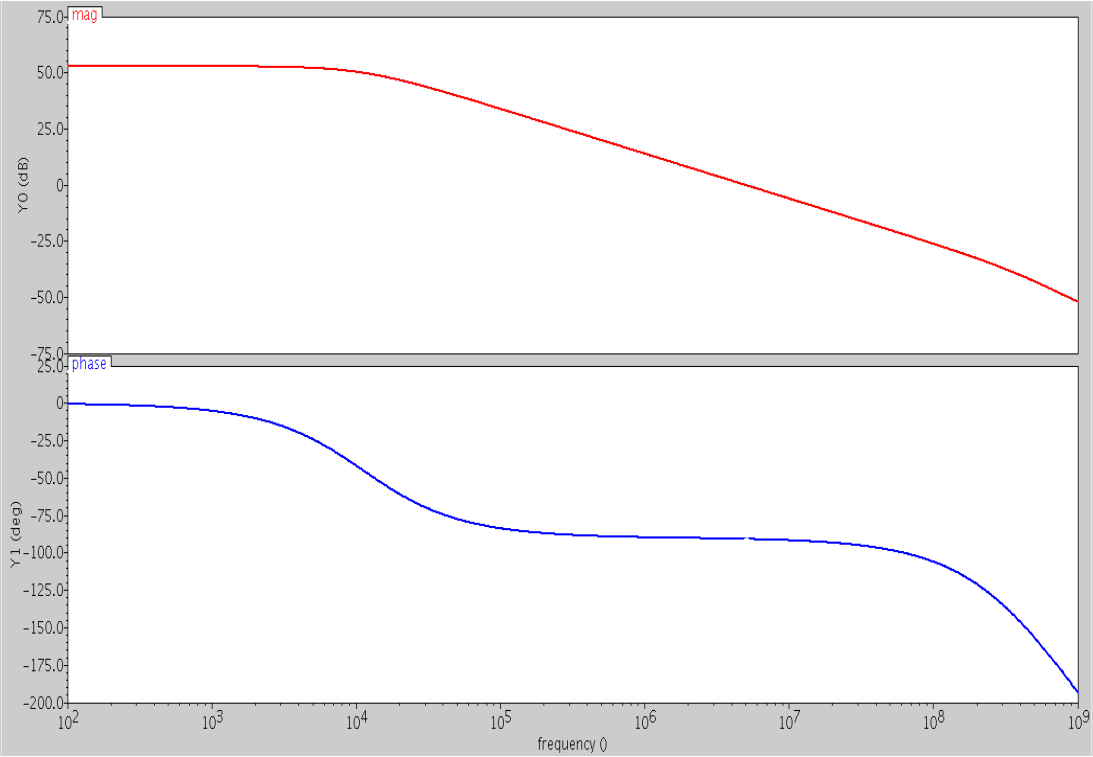


Figure 5.8: AC response of the super inverter

Table 5.2: Performance summary of the super inverter

Vdd	DC gain	GBW	PM	CMRR	PSRR	Current	Process
1.5 V	53 dB	5 MHz	90°	43 dB	45 dB	6.35 µA	0.13 µm

In order to evaluate the variation tolerance of the amplifier, DC and AC corner simulations (Red: nominal; Green: Fast N & Fast P; Yellow: Slow N & Slow P; Blue: Fast N & Slow P; Purple: Slow N & Fast P) have been conducted in Cadence Analog Environment. Due to the positive feedback, imbalance between NMOS and PMOS causes radical change in the large-signal behavior of the amplifier (see blue curves).

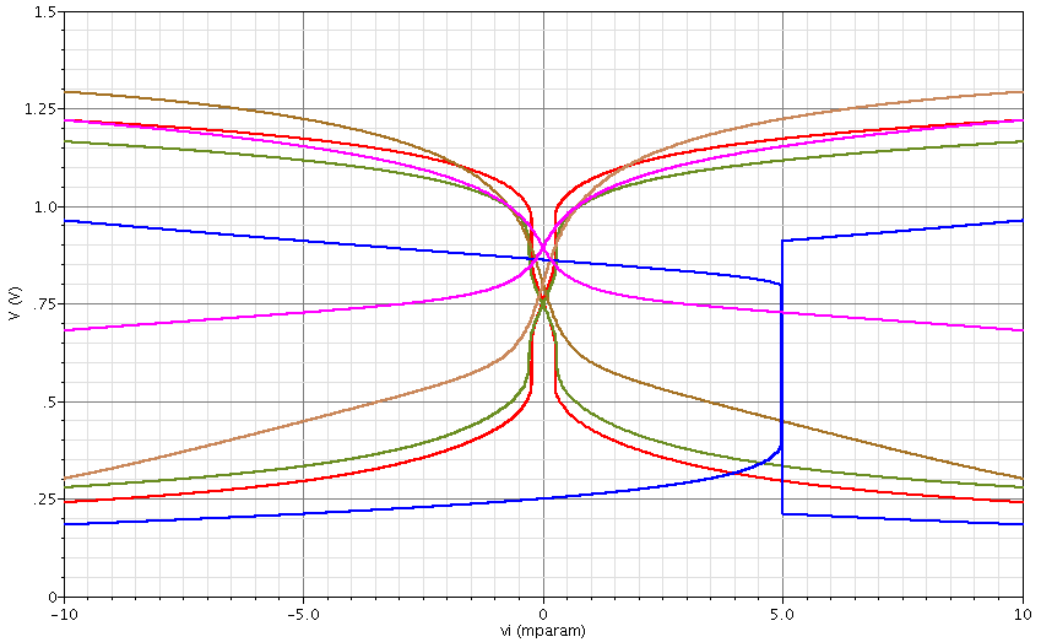


Figure 5.9: Differential-mode DC responses of the super inverter

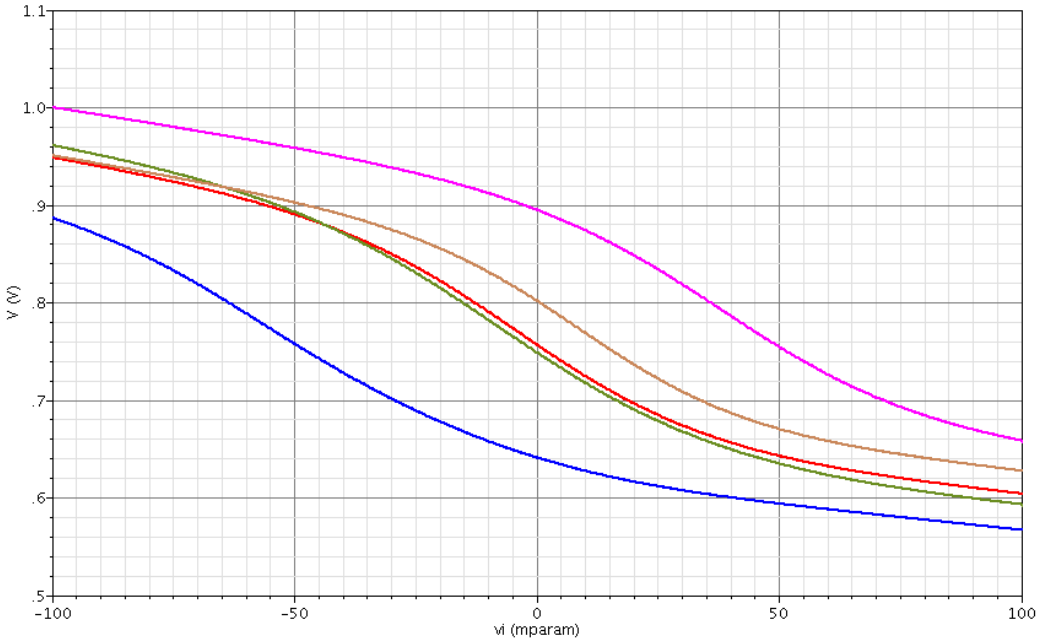


Figure 5.10: Common-mode DC responses of the super inverter

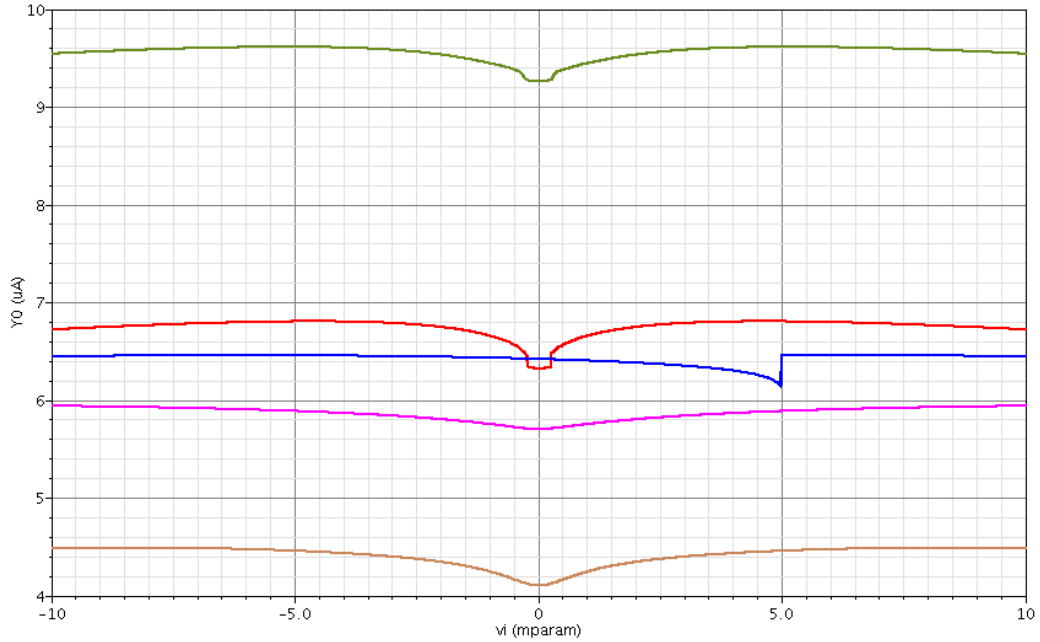


Figure 5.11: DC current variations of the super inverter

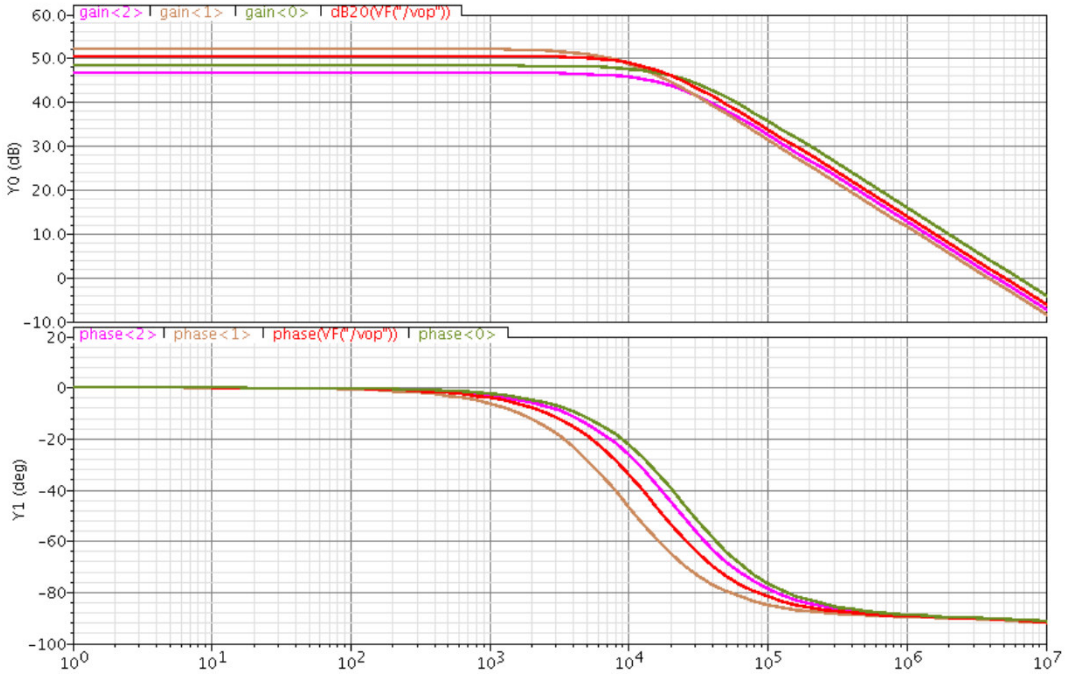
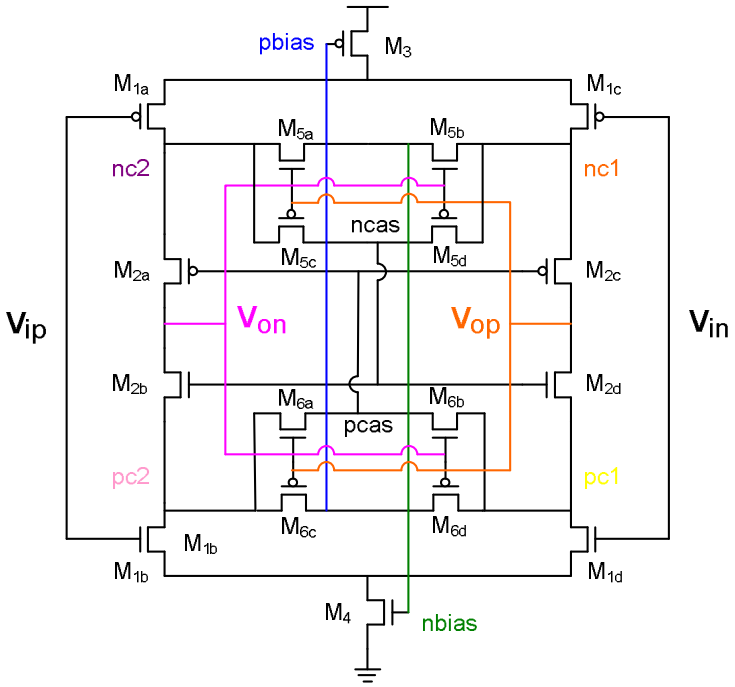


Figure 5.12: AC responses of the super inverter (excluding the “blue” case)

B. The New Inverter

It is seen that the positive feedback loops inside the super inverter limits its linearity and tolerance performance. In addition, the common-mode noise rejection is achieved through modulating a linear MOS device, and the achievable A_{cm} may not be sufficient in some high-precision applications. More internal connections on the output nodes also increase the capacitive loadings, degrading the bandwidth. To mitigate these problems, a modified inverter amplifier topology is devised, as shown in Fig. 5.13. The degenerated input stages of the new inverter are now source-coupled. It also includes a cascode stage to boost the DM gain, but separate common-mode feed back (CMFB) circuits are utilized to bias both the cascode and degeneration stages.



Transistor sizings

$M_{1a,c}$	4.5u/0.24u
$M_{1b,d}$	1.6u/0.24u
$M_{2a,c}$	1.5u/1u
$M_{2b,d}$	0.6u/1u
M_3	1.5u/1u
M_4	0.6u/1u
$M_{5a,b}$	0.72u/0.24u
$M_{5c,d}$	0.72u/0.24u
$M_{6a,b}$	0.72u/0.24u
$M_{6c,d}$	0.72u/0.24u

Figure 5.13: Circuit diagram of the new inverter

1. Operation principles

The operation of this new inverter amplifier lies in the two CMFB circuits, which stabilize the DC operating point and suppress the common-mode noises. Fig. 5.14 shows the top CMFB circuit and the conceptual model, based on two level-shifted MOS resistor pairs. Both PMOS and NMOS sensing circuits are employed to generate level-shifted biasing voltages for the cascode and degeneration stages.

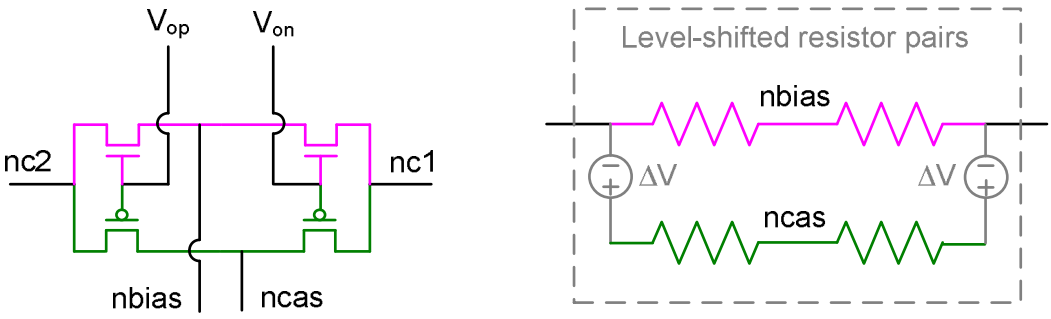


Figure 5.14: CMFB circuit and the conceptual model

For the derivation of the A_{dm}, the node voltages “nbias” and “ncas” can be treated as AC ground. In addition, the drain voltages of the degeneration stages (M_3 and M_4) can also be treated as AC ground due to the differential-mode operation. Given these observations, the A_{dm} of the new inverter should be the same order of magnitude as that of the super inverter. In the CM operation, the CMFB circuit senses the CM variation of the internal voltages. This variation is modulating the gate voltages of both the cascode and the degeneration stages, forming negative feedback loops. In the super inverter, only the degeneration stage is included in the negative feedback. It is therefore that the new inverter amplifier can achieve greater common-mode noise rejection.

2. Simulation results

Fig. 5.15 shows the DC transfer curves of the new inverter. Both differential-mode and common-mode responses are simulated by sweeping the DC input voltage from 0 V to 1.5 V. Obviously, the common-mode response of the new inverter is much more flat in the transition region, which means a high common-mode rejection. Once again, this amplifier also has a rail-to-rail output swing, making it suitable for the applications such as VCO.

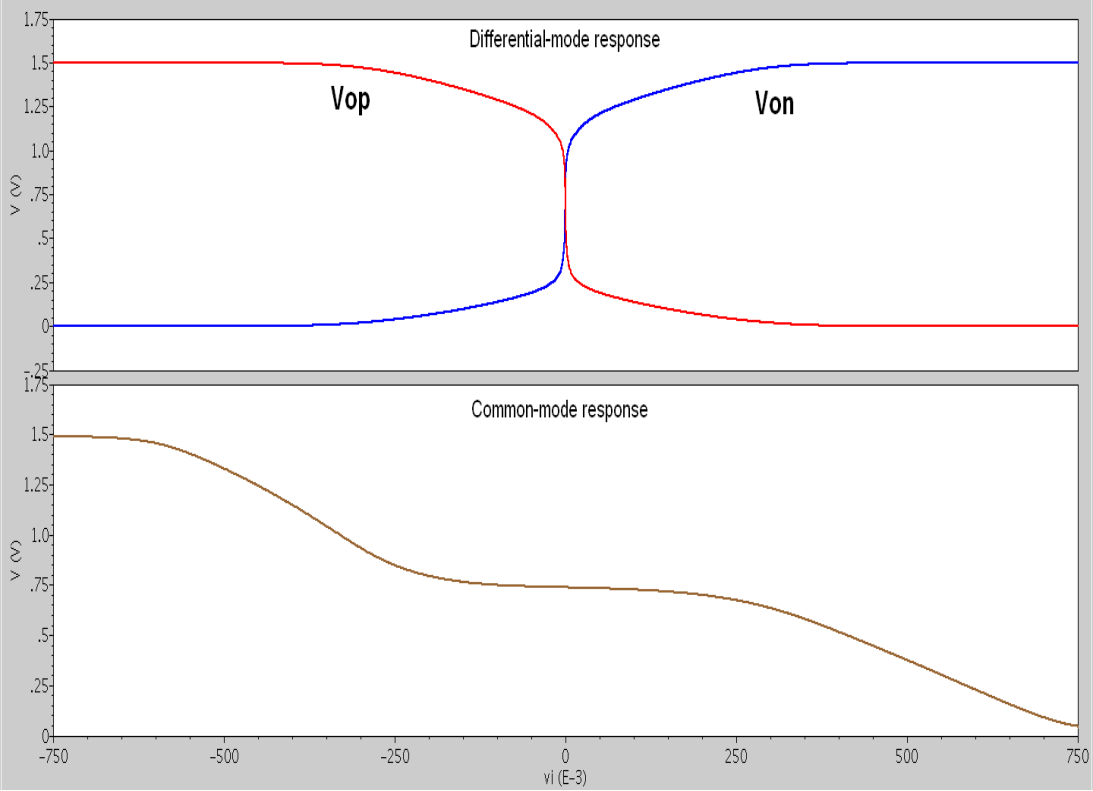


Figure 5.15: DC transfer curve of the new inverter

Fig. 5.16 shows the zoom-in view of the differential-mode DC response, with the differential input swept from -2 mV to 2 mV. Due to the elimination of positive feedback, no sharp transition of the output voltages is seen in the transfer curves. Hence, the new inverter amplifier would produce less harmonic distortion than the super inverter. In addition, the biasing voltages for the differential-mode operation are constant in small-signal variations, verifying the previous discussions.

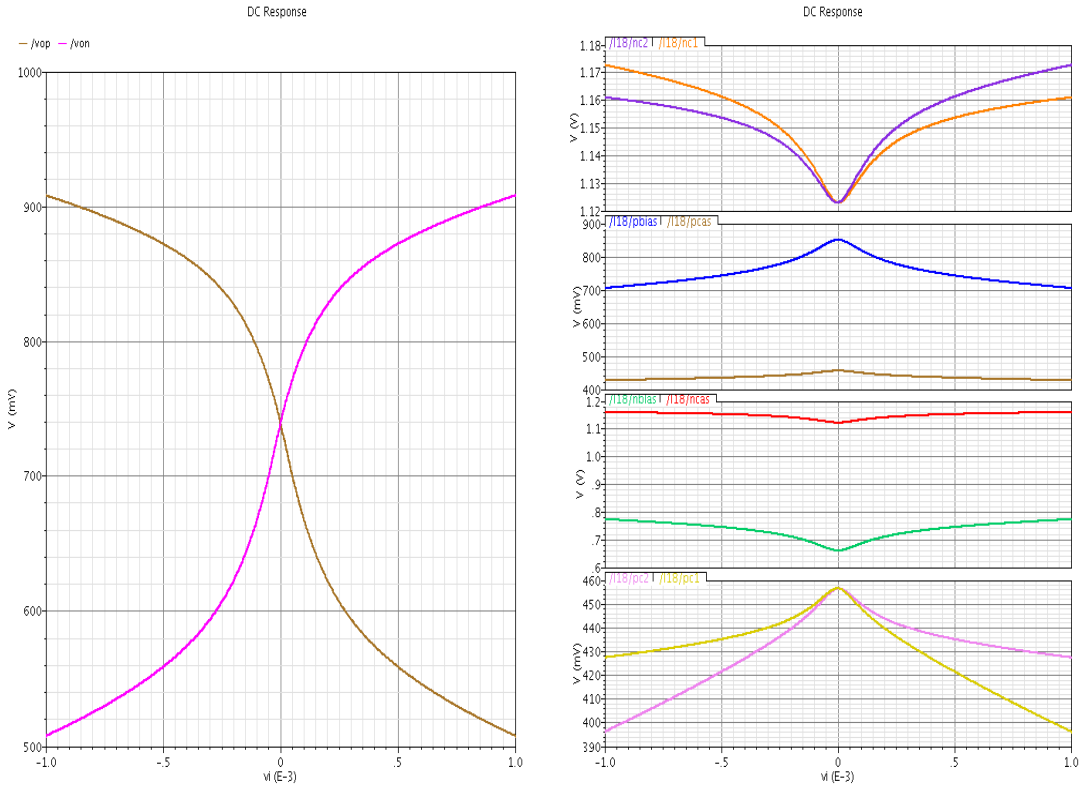


Figure 5.16: Zoom-in view of the DC response

Table 5.3 summarizes the simulated characterizations of the new inverter at 1.5 V supply. Fig. 5.17 compares the DC responses between the two inverter amplifiers. The new inverter amplifier shows better current efficiency and linearity.

Table 5.3: Performance summary of the new inverter

Vdd	DC gain	GBW	PM	CMRR	PSRR	Current	Process
1.5 V	58 dB	4.8 MHz	90°	80 dB	65 dB	1.6 µA	0.13 µm

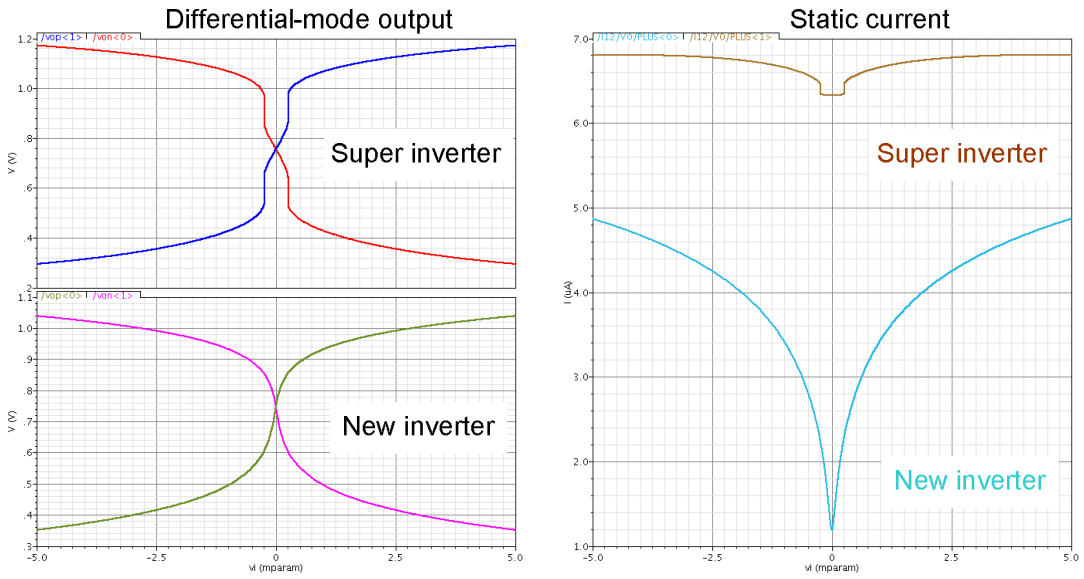


Figure 5.17: Differential-mode DC comparisons

The following figures show the different corner simulations, with the same color codes. Since the new inverter has higher CM rejection, its static current shows less variation across the corners, compared to the super inverter. Due to the voltage-limited operation, a self-biased amplifier usually shows large static-current variation. In addition, there is no positive feedback in the new inverter, and hence its large-signal behavior is more stable and no radical change occurs in the DC response.

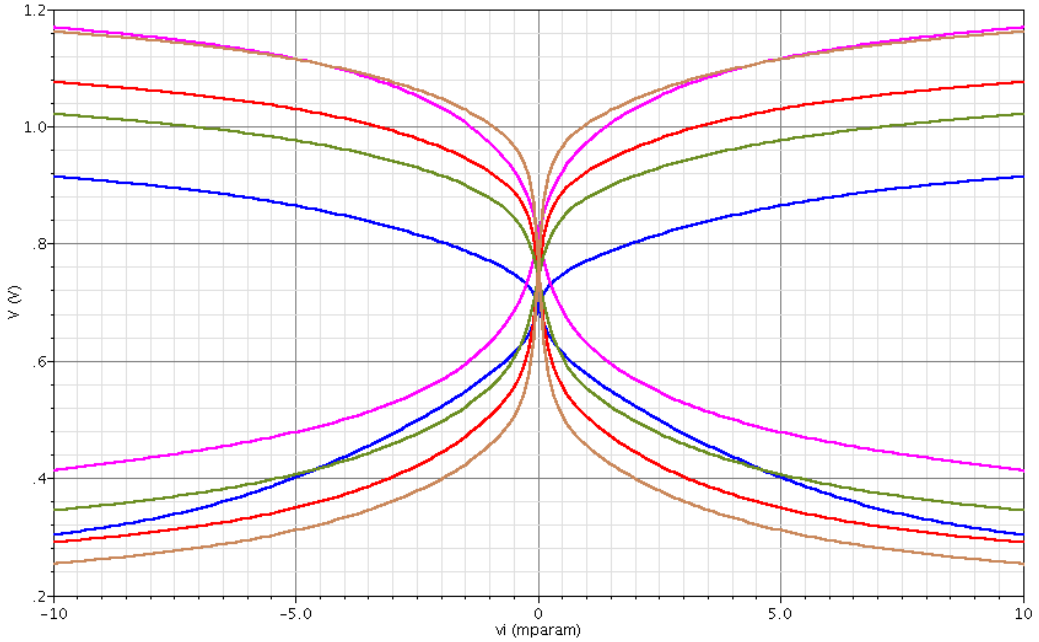


Figure 5.18: Differential-mode DC responses of the new inverter

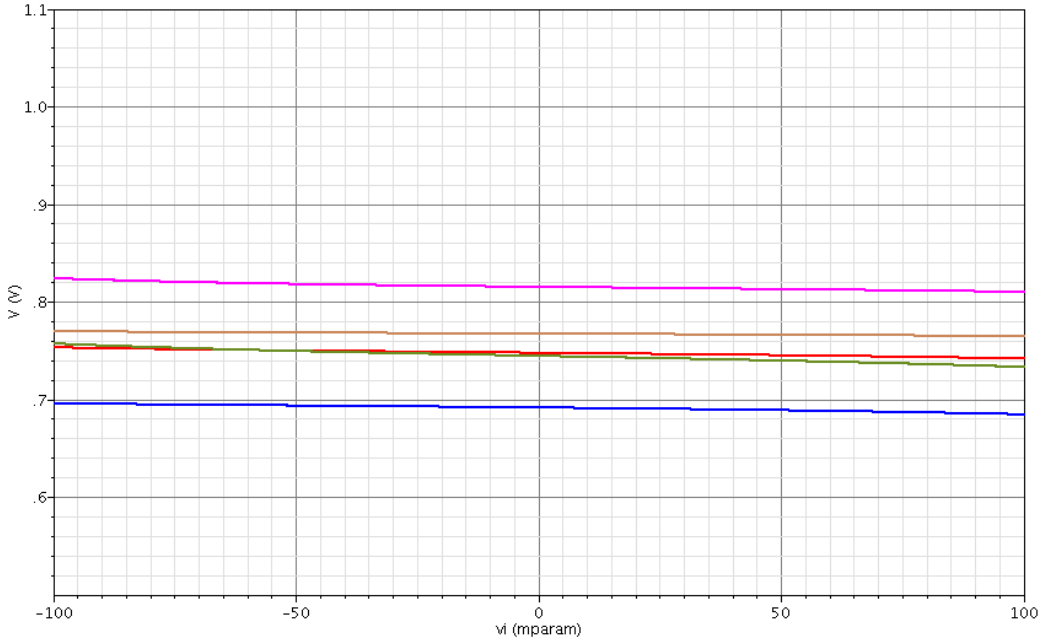


Figure 5.19: Common-mode DC responses of the new inverter

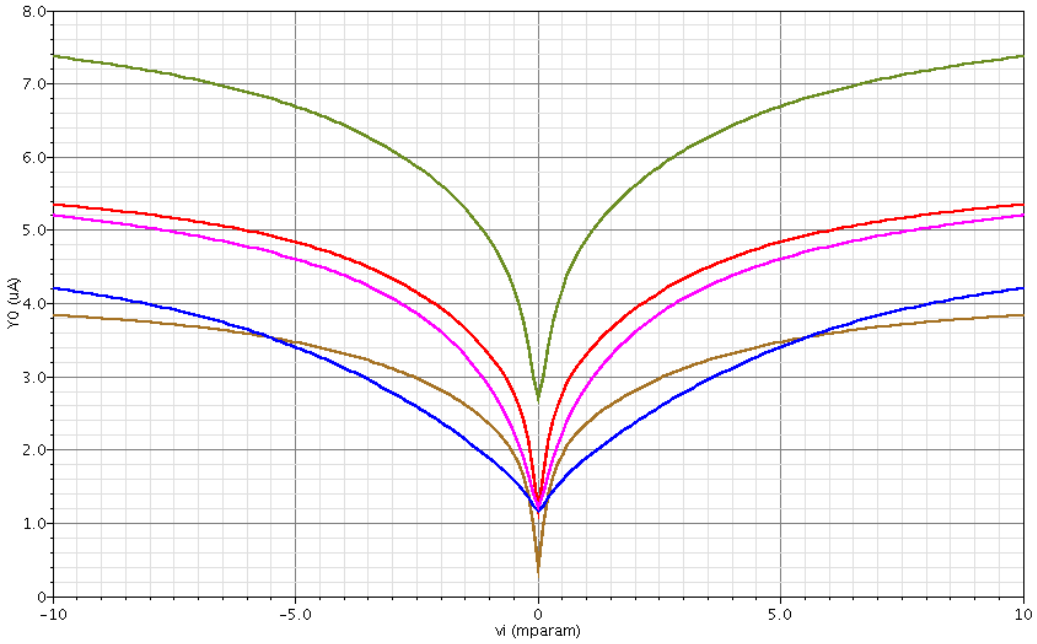


Figure 5.20: DC current variations of the new inverter

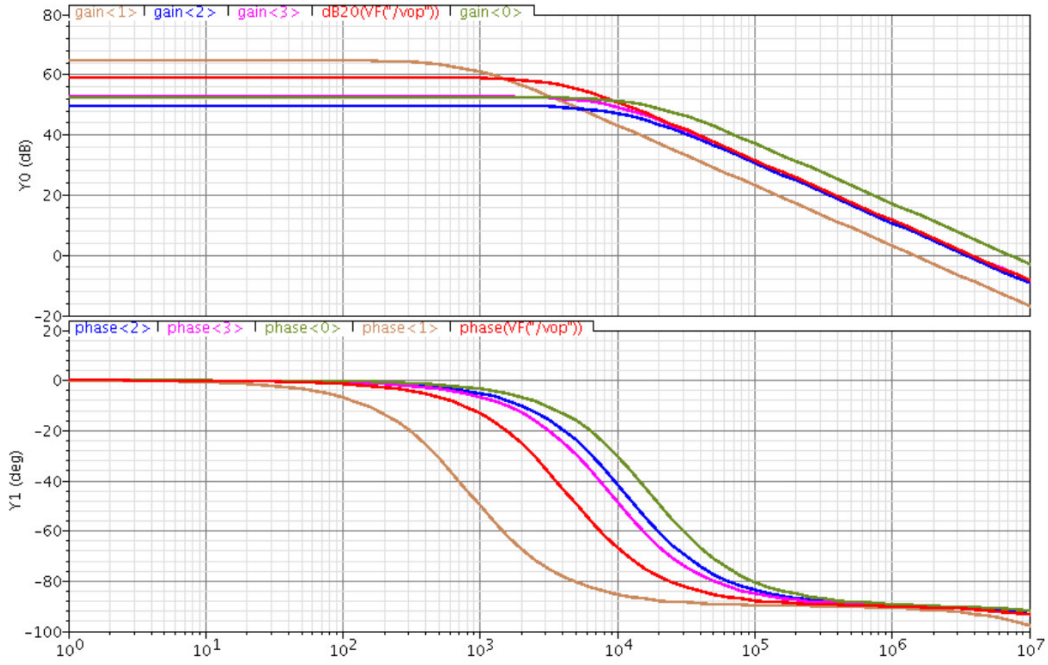


Figure 5.21: AC responses of the new inverter

The following figures show the Monte-Carlo analysis of the A_{dm} and A_{cm} under process variation and mismatch, and tight variation distribution is achieved.

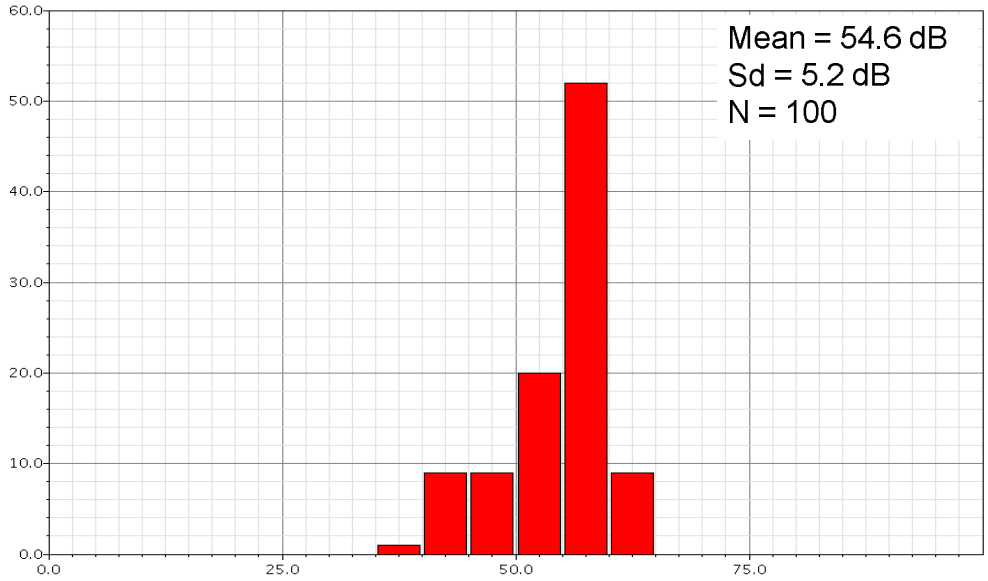


Figure 5.22: Process variation on the A_{dm} of the new inverter

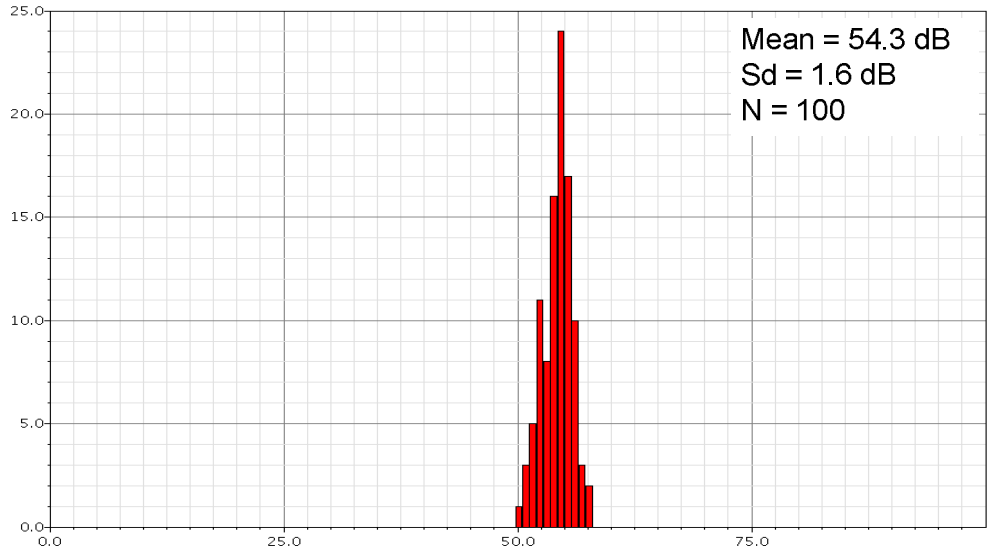


Figure 5.23: Mismatch analysis on the A_{dm} of the new inverter

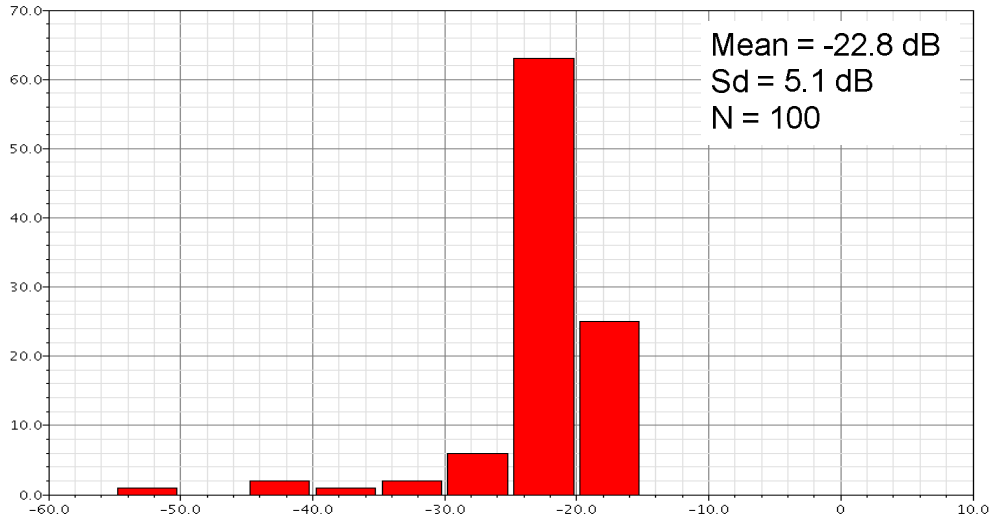


Figure 5.24: Process variation on the A_{cm} of the new inverter

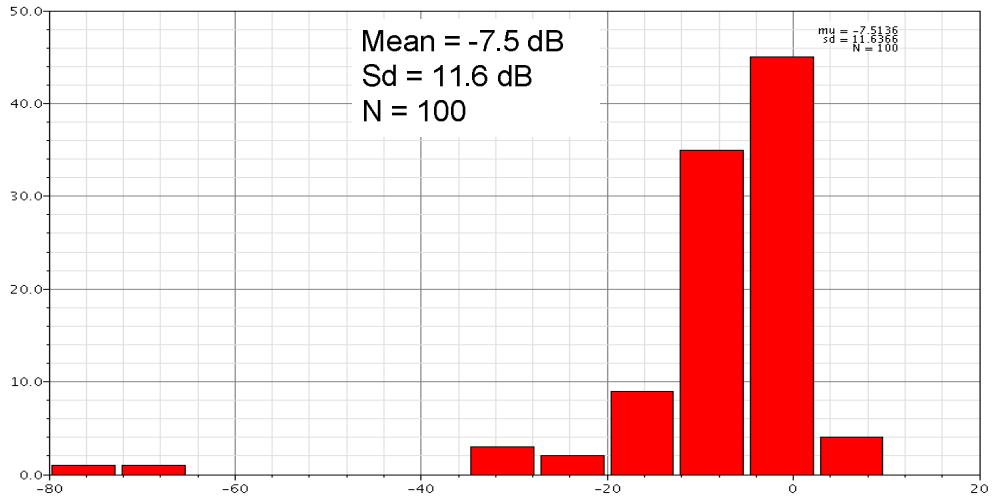
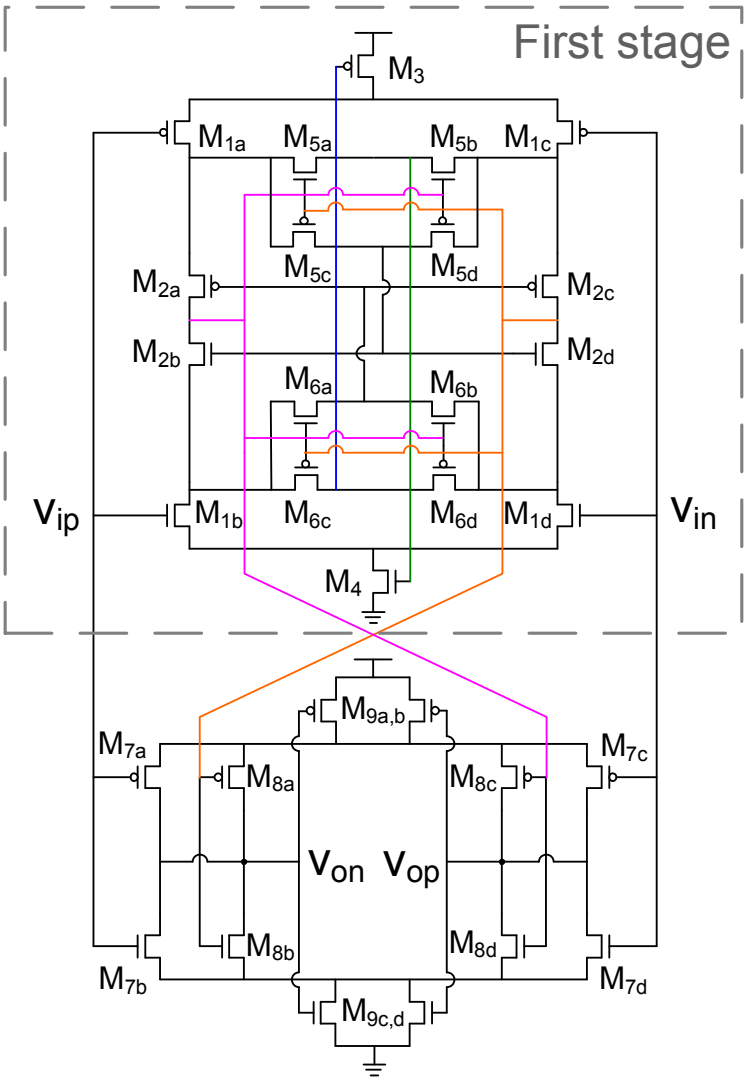


Figure 5.25: Mismatch analysis on the A_{cm} of the new inverter

3. High-gain topology

To further boost the DC gain, a high-gain inverter is also proposed based on the new inverter amplifier, as shown in Fig. 5.26. To adjust the phase response without employing miller capacitors, feedforward compensation is utilized by feeding both the input and the output of the first stage feed into the second stage [Sansen90].



Transistor sizings

$M_{1a,c}$	4.5u/0.24u
$M_{1b,d}$	1.6u/0.24u
$M_{2a,c}$	1.5u/1u
$M_{2b,d}$	0.6u/1u
M_3	1.5u/1u
M_4	0.6u/1u
$M_{5a,b}$	0.72u/0.24u
$M_{5c,d}$	0.72u/0.24u
$M_{6a,b}$	0.72u/0.24u
$M_{6c,d}$	0.72u/0.24u
$M_{7a,c}$	9u/0.54u
$M_{7b,d}$	3.2u/0.54u
$M_{8a,c}$	9u/1u
$M_{8b,d}$	3.2u/1u
$M_{9a,b}$	3u/1u
$M_{9c,d}$	1.5u/1u

Figure 5.26: Circuit diagram of the high-gain inverter amplifier

Fig. 5.27 gives the zoom-in view of the differential-mode DC response of the high-gain inverter amplifier. It shows not only higher gain but also better linearity performance in the transition region. Fig. 5.28 plots the AC response, and the simulation characterizations are summarized in Table 5.4. In MASH architectures, this level of accuracy is usually required for the amplifier employed in the loop filter.

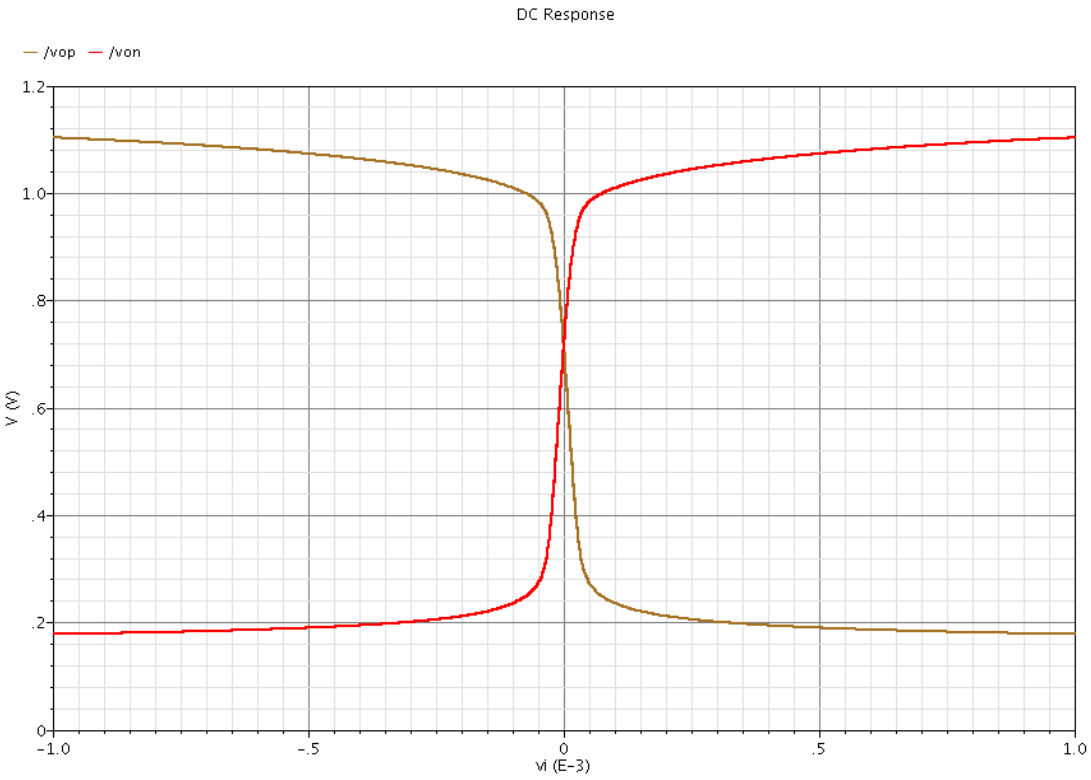


Fig. 5.27: DC response of the high-gain inverter amplifier

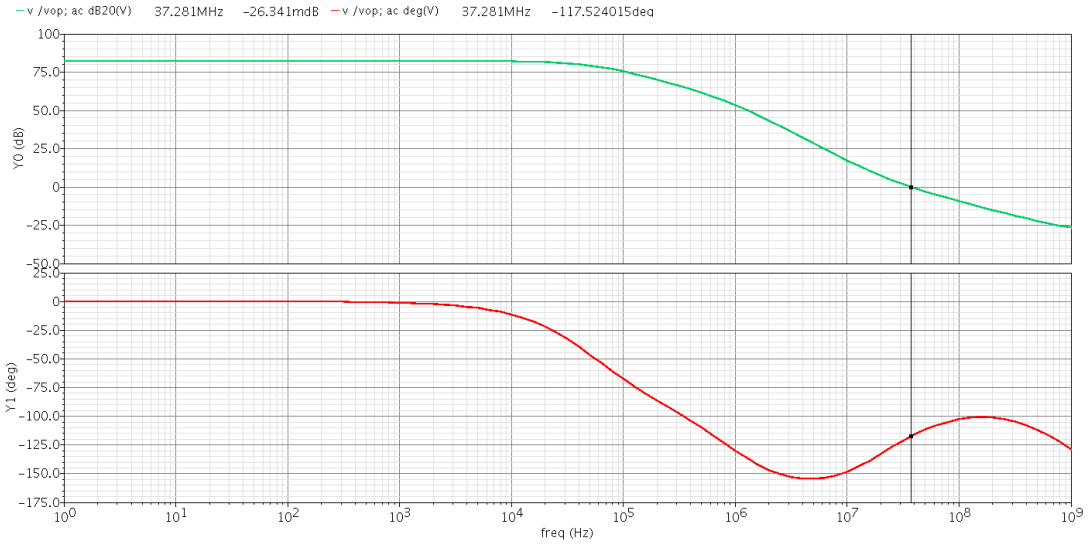


Fig. 5.28: AC response of the high-gain inverter amplifier

Table 5.4: Performance summary of the high-gain inverter amplifier

Vdd	DC gain	GBW	PM	CMRR	PSRR	Current	Process
1.5 V	82 dB	37 MHz	63^{o}	98 dB	88 dB	12 µA	0.13 µm

C. Floating CDS

To boost the gain performance of the inverter amplifier while also optimizing the power efficiency, correlated double sampling (CDS) technique is investigated. Theoretically, CDS technique doubles the effective gain of an amplifier in the dB scale with slightly more area and power consumption [Temes96]. Fig. 5.29 shows a single-ended SC integrator with the CDS circuit, driven by non-overlapping clocks.

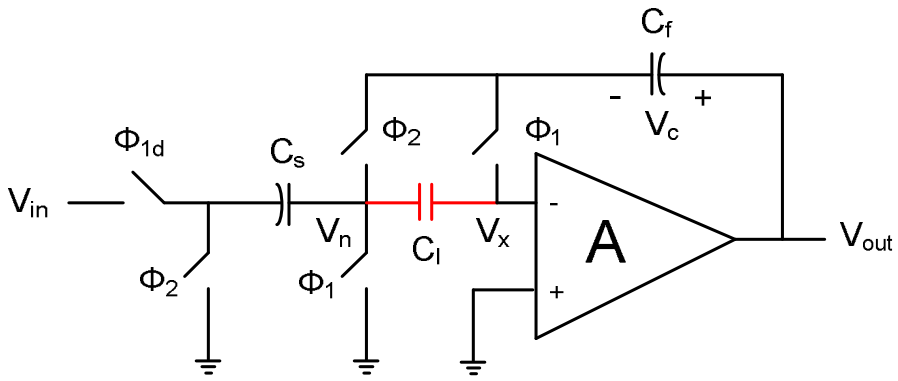


Fig. 5.29: A single-ended SC integrator with CDS

During phase Φ_1, the integrator samples the input signal, and the integration capacitor (C_f) closes the amplifier in a negative feedback. Assuming the voltage across C_f is $V_c[n]$, the error voltage (V_x) at the amplifier input can be found, as shown in Eq. 5.7. This voltage will be stored on the floating capacitor (C_l).

$$V_x = -\frac{V_c[n]}{1+A} = -\frac{V_c[n]}{A(1+1/A)} \approx -V_c[n]\cdot\left(\frac{1}{A}-\frac{1}{A^2}\right) \tag{5.7}$$

During phase Φ_2, the circuit transfers the charges. V_n serves as the new virtual ground, and V_x will assume a value given by Eq. 5.8. If $V_c[n]$ and $V_c[n+1]$ are the same, the small change on V_x is given by Eq. 5.9. Since the floating capacitor is in

series with the amplifier input port, the steady-state voltage of V_n will be very close to ground. Thus, a much more accurate integrator can be realized with a relatively low gain amplifier, and the transfer function of the SC integrator is given by Eq. 5.10.

$$V_x \approx -V_c[n+1]\cdot\left(\frac{1}{A}-\frac{1}{A^3}\right)\approx -V_c[n+1]\cdot\frac{1}{A} \tag{5.8}$$

$$V_n = \Delta V_x = -V_c[n+1]\cdot\frac{1}{A^2} \tag{5.9}$$

$$H(Z)=\frac{V_o(Z)}{V_i(Z)}=\frac{C_s}{C_f}\frac{1}{Z\left(1+\frac{C_s/C_f}{A^2}\right)-1} \tag{5.10}$$

Aside from the high-gain merit, the CDS technique can also store the DC offset and flicker noise of the amplifier onto the floating capacitor, since any input-referred low frequency error of the amplifier will be high-pass filtered to the first order. In addition, the amplifier nonlinearity is also cancelled as well, and the output harmonic distortion of the integrator would be greatly suppressed.

However, the CDS technique heavily relies on the correlation between the two successive output voltages. Any difference affects the resulting accuracy of the error cancellation [Grilo98]. Due to the chaotic nature of the delta-sigma modulator, the internal states change radically from cycle to cycle even though oversampling is assumed, thus the conventional CDS topology cannot be directly applied in the modulator design. In this section, a floating CDS topology, which utilizes two sets of capacitors in a time-interleaved fashion, is presented for accommodating the low-gain inverter amplifier in a MASH modulator design.

1. Floating sampling scheme

Before introducing the CDS topology, the floating sampling scheme, which is used for self-referencing the SC integrator, will be firstly discussed. As mentioned previously, the inverter amplifiers have a narrow input CM range due to the voltage-biasing. It is therefore necessary to decouple the input CM voltage and the nominal DC biasing voltage of the amplifier. Fig. 5.30 shows the floating sampling topology in an inverter amplifier-based SC integrator. Pseudo-resistor is utilized to setup the input DC conditions for the amplifier, and it will be explained in detail in the next chapter.

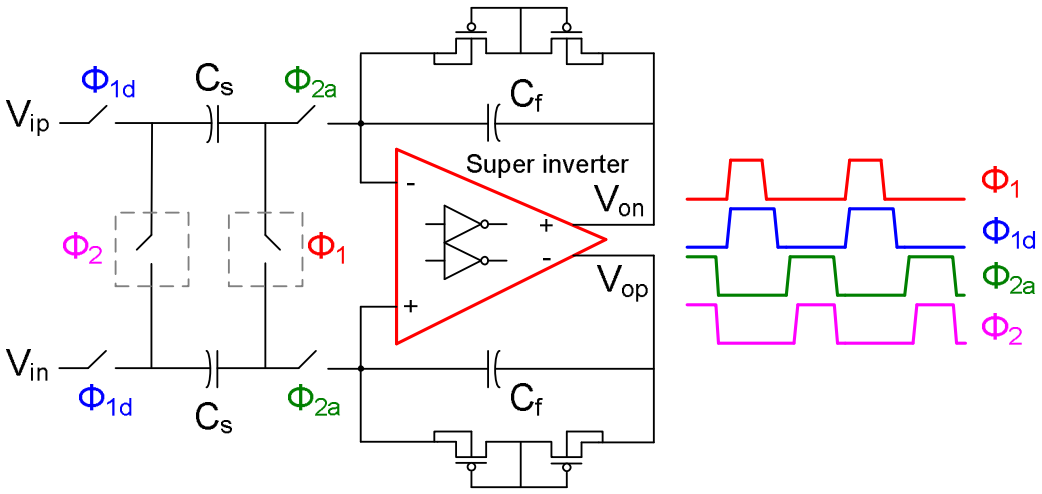


Fig. 5.30: A floating fully-differential SC integrator

Fig. 5.31 illustrates the step-by-step operations of this floating SC integrator. During phase Φ_1, the floating node V_x tracks the input CM voltage, and only differential charges are stored onto the sampling capacitors, shown in Eq. 5.11 and 5.12. The bottom plate sampling technique is used to eliminate the input-dependent

charge injection. During phase Φ_2, the sampling capacitors are first boot-strapped to the nominal DC biasing voltage (V_{cm}) of the amplifier by closing the Φ_{2a} switch in advance. It is important to stabilize the DC biasing conditions for the inverter amplifier. Otherwise, the input/output CM level of the integrator may drift over time, walking the amplifier away from its transition region. Finally, the Φ_2 switch is closed to finish the integration.

$$V_{ip} - V_x = V_{ip} - \frac{V_{ip} + V_{in}}{2} = \frac{V_{ip} - V_{in}}{2} \tag{5.11}$$

$$V_{in} - V_x = V_{in} - \frac{V_{ip} + V_{in}}{2} = -\frac{V_{ip} - V_{in}}{2} \tag{5.12}$$

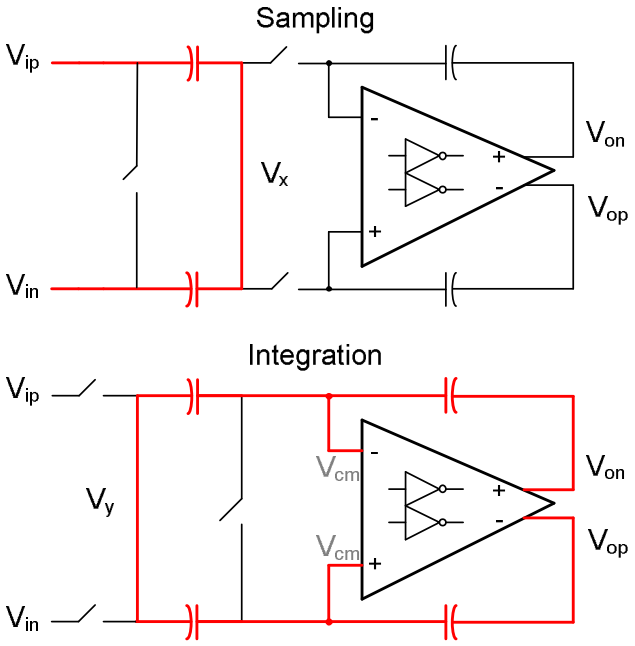


Fig. 5.31: Operation steps of the floating SC integrator

2. The CDS topology

Fig. 5.32 shows a SC integrator incorporating the floating CDS circuit. In this integrator, two sets of sampling and feedback capacitors are utilized to force the correlation between the two signal paths. C_{sm} and C_{fm} form the main path for the integration, and C_{ss} and C_{fs} form the secondary path to estimate the next output state of the main path. There two paths operate in a time-interleaved manner: when the main path samples the input signal, the secondary path performs the integration, and vice versa. Hence, no additional clock phase is required to handle the extra signal processing, and this circuit can run at roughly the same speed as the conventional SC integrator.

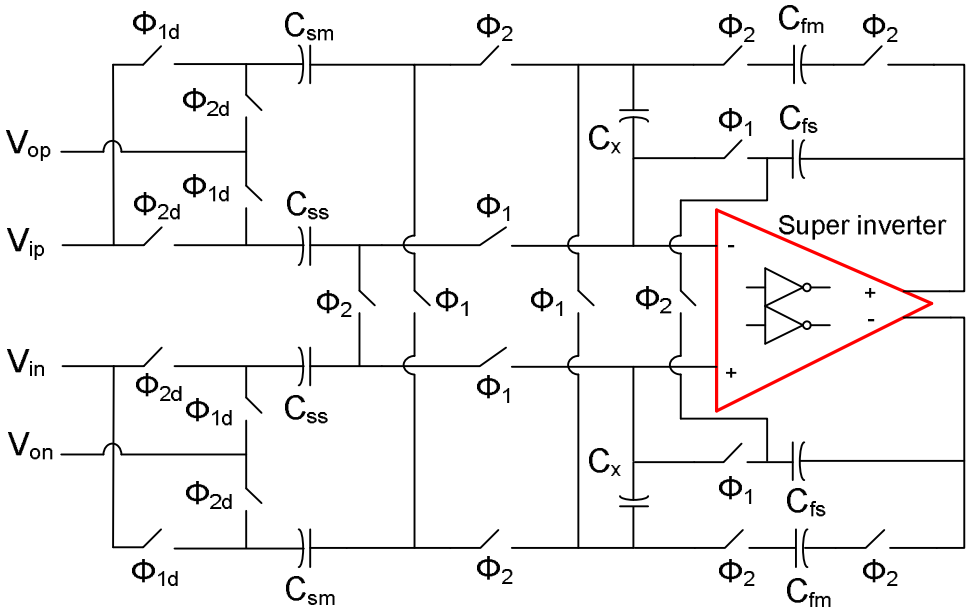


Fig. 5.32: SC integrator incorporating the floating CDS circuit

Fig. 5.33 shows the simplified view of the two-path SC integrator in phase Φ_1. During phase Φ_1, the main path samples the input signal and the secondary path transfers the charges. At the same time, the differential error voltage of the inverter amplifier will be stored onto the two floating capacitors C_x. The floating nodes of C_x are tied together and will be boot-strapped to the nominal DC biasing voltage of the amplifier. For the next clock phase, the floating nodes form a much more accurate virtual ground for the integration of the main path. To achieve that goal, Eq. 5.13 also needs to be followed in designing the capacitors.

$$\frac{C_{sm}}{C_{fm}} = \frac{C_{ss}}{C_{fs}} \tag{5.13}$$

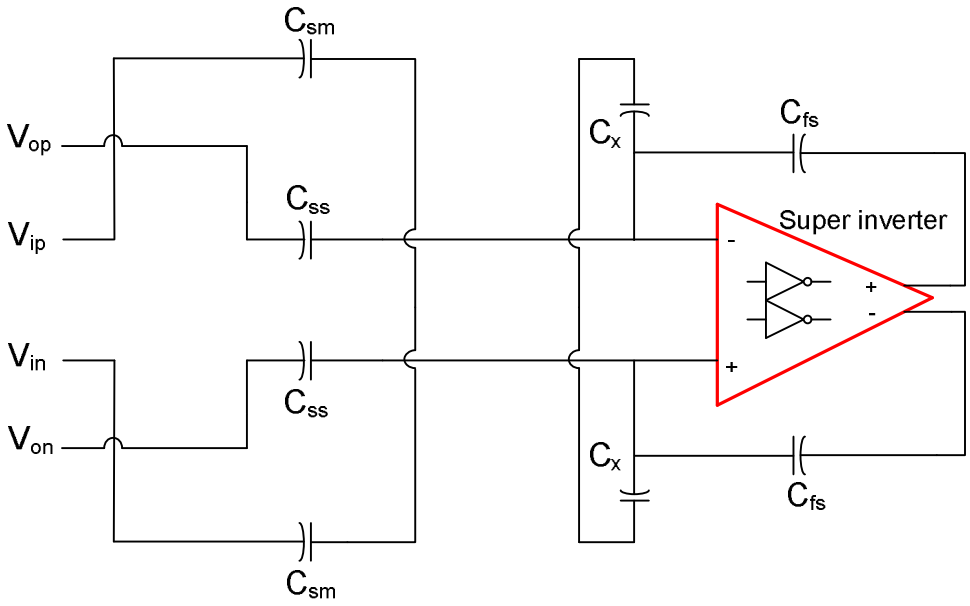


Fig. 5.33: The two-path SC integrator in phase Φ_1

Fig. 5.34 shows the simplified view of the two-path SC integrator in phase Φ_2. During phase Φ_2, the secondary path samples the input signal, and the main path performs the integration. C_x is now in series with the amplifier input ports, and the stored error voltage cancels the amplifier nonidealities to the first order. In the mean while, the left plates of the secondary feedback capacitors are shorted together, and their differential voltage will be updated by the output state of the main path.

It is critical to force the correlation between the two paths. Without this step, the difference in the output states of the two paths would drift over time, disabling the CDS. Due to the oversampling, the successive input samples into the two paths will be very close. In addition, V_{op} and V_{on} will also be arranged the same for the whole clock cycle. Therefore, the secondary path can always estimate the next output state of the main path and store the appropriate error voltage onto the floating capacitors.

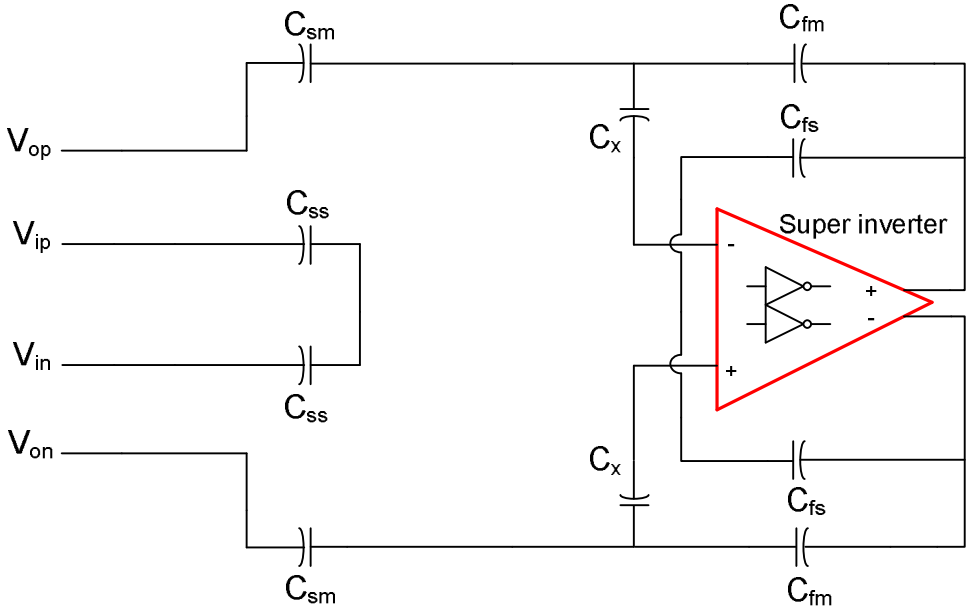


Fig. 5.34: The two-path SC integrator in phase Φ_2

3. Performance evaluation

Fig. 5.35 shows the simulated transient responses at the new virtual grounds and amplifier outputs of the two-path SC integrator. Clearly, the two output states of the integrator are very close in a clock cycle. The first one (in phase Φ_1) is the estimation step of the secondary path; the second one (in phase Φ_2) is the actual integration of the main path. By measuring the steady-state differential output and input voltages, the effective DC gain of the amplifier can be calculated. It shows that the effective gain is around 80 dB, realizing 20-30 dB gain-boosting.

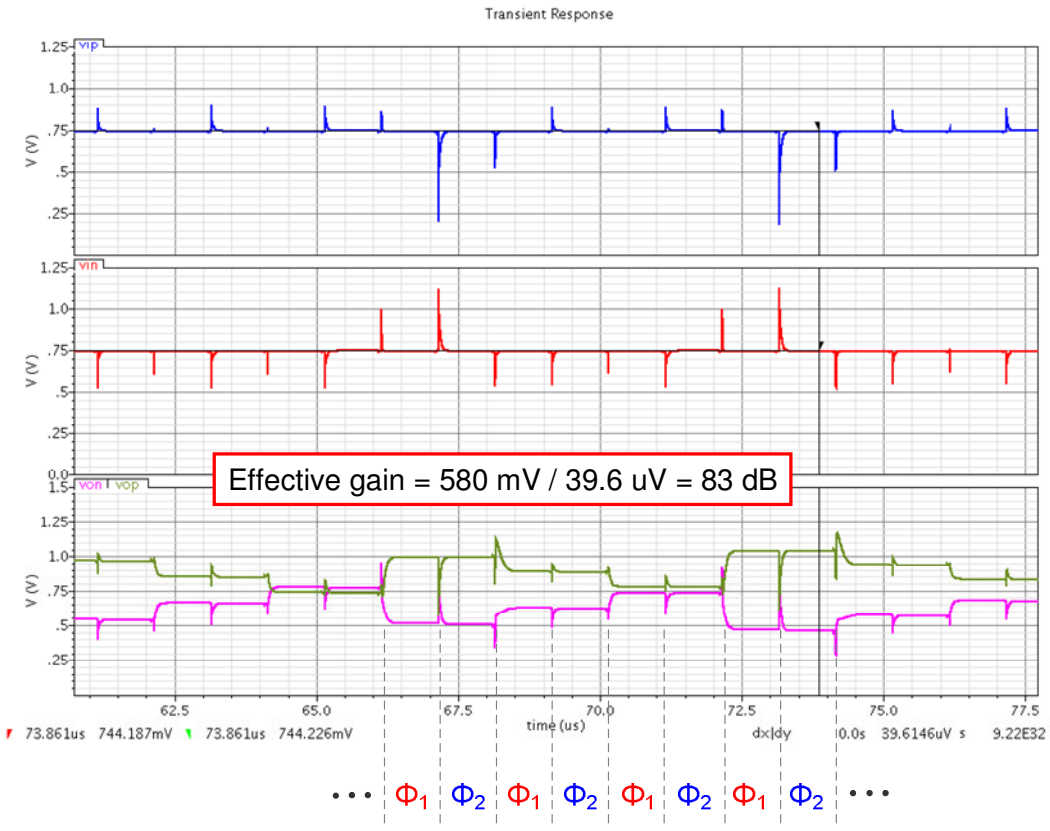


Fig. 5.35: Transient response of the two-path SC integrator

Aside from addressing the finite gain effect, a more thorough simulation will reveal that the floating CDS technique can also mitigate the nonlinear gain effect, and this is also important for the delta-sigma modulator design. On the other hand, there are several practical drawbacks that limit the effectiveness of the CDS technique, as listed in the following.

1. Additional set of capacitors produces more input-referred KT/C noise in the ADC. The increased KT/C noise should not degrade the overall noise improvement.
2. Charge injection makes it necessary to employ a big floating capacitor. In this design, C_x has the same size as C_{fm}. However, this reduces the settling accuracy of the secondary path and therefore the achievable gain-boosting.
3. More capacitive loadings increase the power consumption of the amplifier and the overall silicon overhead. Since the secondary path is only for estimation, the capacitor values of C_{ss} and C_{fs} can be scaled down proportionally.
4. The output states are divided into two clock cycles. Hence, the output state of the main path has to feed into the next stage during the same clock phase. This not only increases the capacitive loading for the main path, but also complicates the overall timing arrangements.
5. As the input amplitude increase, the increased difference in the successive input samples into the two paths would degrade the accuracy of the error cancellation. Therefore, the SNR/SNDR of the delta-sigma modulator with the CDS circuit may roll off as the input amplitude approaches the full-scale.

VI. CHIP IMPLEMENTATION

This chapter presents the chip implementation of the inverter amplifier-based delta-sigma modulators at the system, circuit, and layout levels.

A. System Level Design

The modulator topology needs to be verified in a behavioral simulator such as Simulink, based on which the modulator parameters can be determined and the performance limitations can be identified. In the dissertation, both the 2nd-order delta-sigma modulator and 4th-order MASH modulator have been prototyped. This section discusses both system designs.

1. Simulink models

Fig. 6.1 shows the simulink model for the 2nd order modulator. In this model, the SD toolbox is utilized and the integrator nonidealities and the KT/C noise are also considered [Malcovati03]. The internal states can be probed to detect the integrator overloading.

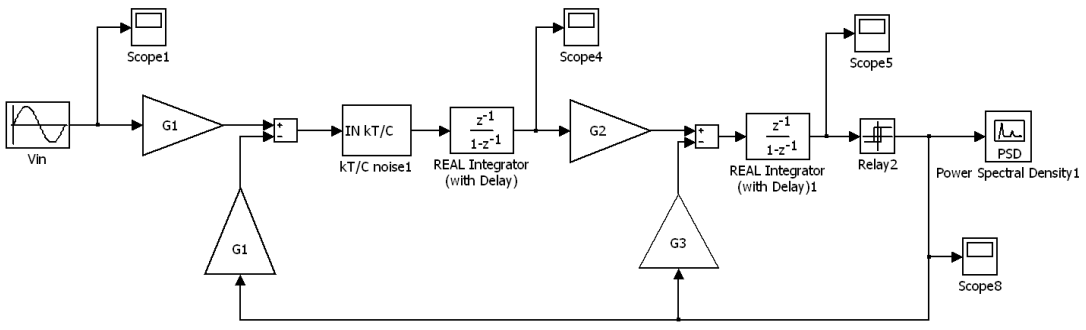


Fig. 6.1: Simulink model of the 2nd-order modulator

The Boser-Wooley structure is chosen for the 2nd-order modulator design. Since two delaying SC integrators are used in this structure, it allows the Opamp in each integrator to settle independently of each other, therefore relaxing the speed requirements [Boser88]. To increase the dynamic range of the modulator, the low distortion Silva-Steensgaard structure, distinguished by the direct feedforward path from the input to the quantizer, may also be used [Silva01]. Therefore, the input signal to the loop filter only contains the shaped quantization noise, and the linearity requirement on the Opamp is greatly reduced.

The DT delta-sigma modulator has been prototyped in the dissertation for several reasons. First, the insensitivity of the DT modulator to process variations eliminates the need for any tuning circuitry, thereby reducing the system complexity. Second, the loop filter scalability with the clock makes the DT modulator more flexible for different SNR targets. In the measurement, the clock frequency can be easily optimized for the tradeoff between resolution and power consumption. Third, the inherent accuracy of the loop filter coefficients makes it straightforward to extend the single-stage modulator to higher order MASH architecture. Finally, due to the input DC biasing issue, the inverter amplifiers are more suitable for the implementation of SC circuits.

A single-bit quantizer is employed in the modulator prototypes for the simplicity and inherent linearity. As discussed in Chapter IV, no digital correction logic is required for the single-bit modulator to trim the DAC nonlinearity. This greatly reduces the system complexity and power consumption.

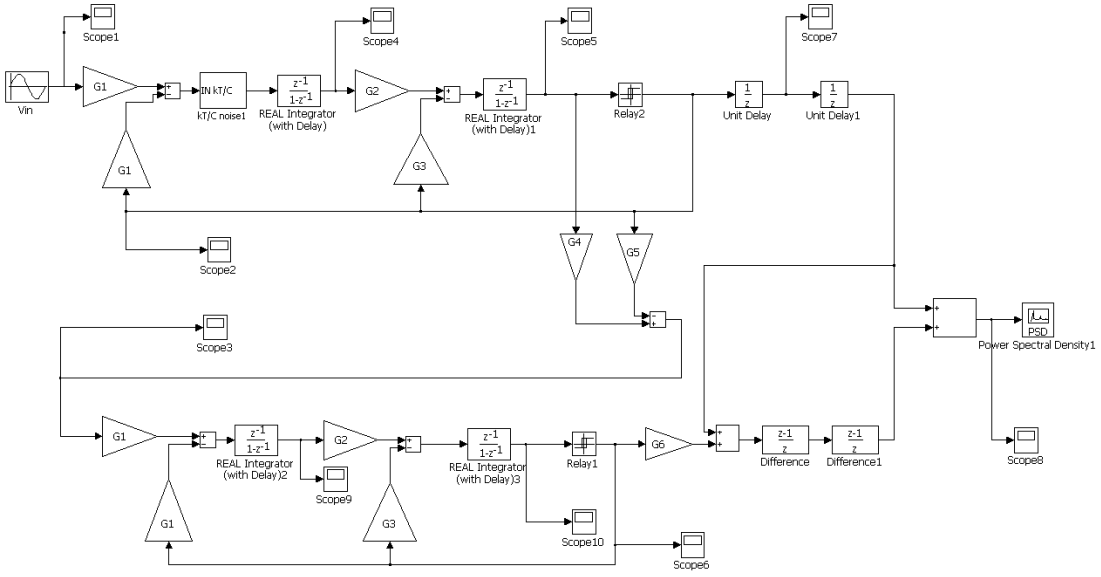


Fig. 6.2: Simulink model of the 4th-order MASH

Fig. 6.2 shows the simulink model for the 4th-order MASH architecture. Two stages of 2nd order modulators are cascaded to achieve the higher order noise shaping. The quantization noise from the first modulator is scaled down before feeding into the second modulator. Without proper scaling, the total input signals to the second modulator would be near the full-scale, causing integrator overloading. The second modulator output can then be scaled up before the digital cancellation. In addition, the scaling factor for the first modulator output (G_5) is doubled for achieving a more realistic capacitor value. To account for this, a compensation path adds the delayed output of the first modulator to the output node of the second modulator.

The 4th order MASH may also be implemented in a 2-1-1 structure to reduce the scaling factor (G_6). Since three stages are cascaded, the mismatch between them may actually result in more in-band noise at the output.

2. Choice of the modulator parameters

Table 6.1 gives the values for the 2nd-order modulator parameters. Fig. 6.3 shows the simulink spectrum of the modulator based on a 32000-point DFT. The Opamp nonlinearity is not included in the simulation, and the actual SNR/SNDR performance would be 5-10 dB lower than the simulation.

Table 6.1: 2nd-order modulator parameters

G1	G2	G3	BW	OSR	C_s	Ampl	N
1/4	2/3	1/3	8 KHz	100	0.1 pF	-12 dBFS	32K

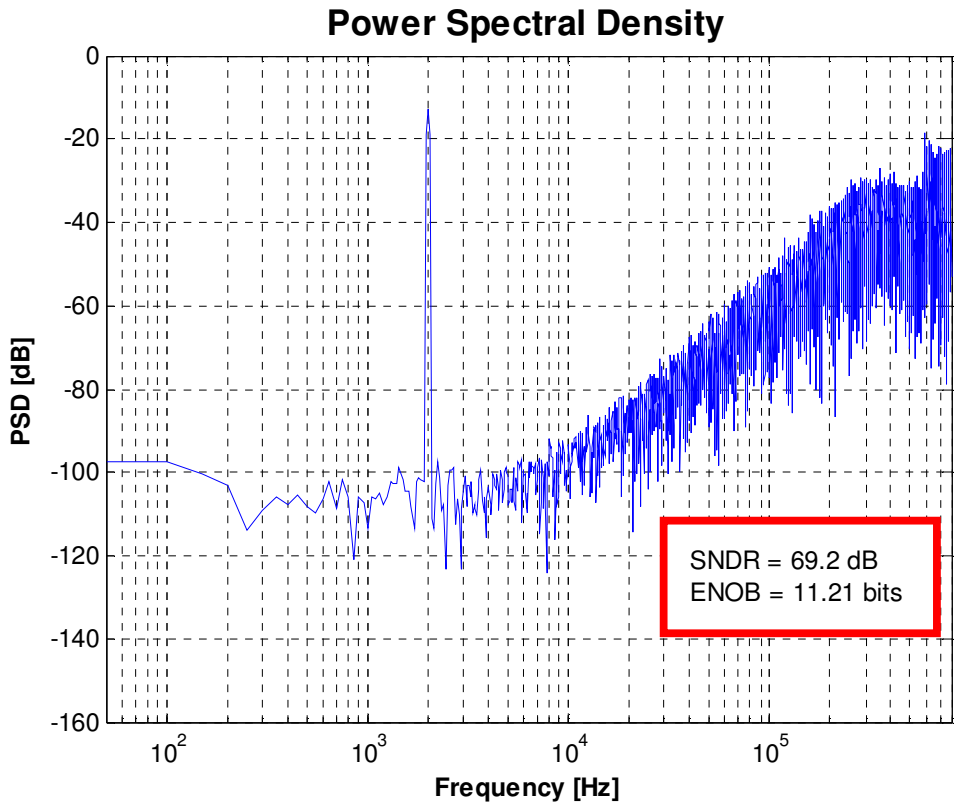


Fig. 6.3: Simulink spectrum of the 2nd-order modulator

Table 6.2 gives the values for the 4th-order MASH parameters. Fig. 6.4 shows the simulink spectrum of the MASH based on a 32000-point DFT. Since CDS is included in the MASH prototypes to address the nonlinearity effects, the measured resolution can be accurately predicted by the simulation.

Table 6.2: 4th-order MASH parameters

G1	G2	G3	G4	G5	G6	BW	OSR	Cs	Ampl	N
1/4	2/3	1/3	1	1/3	6	20 KHz	64	0.2 pF	-12 dBFS	32K

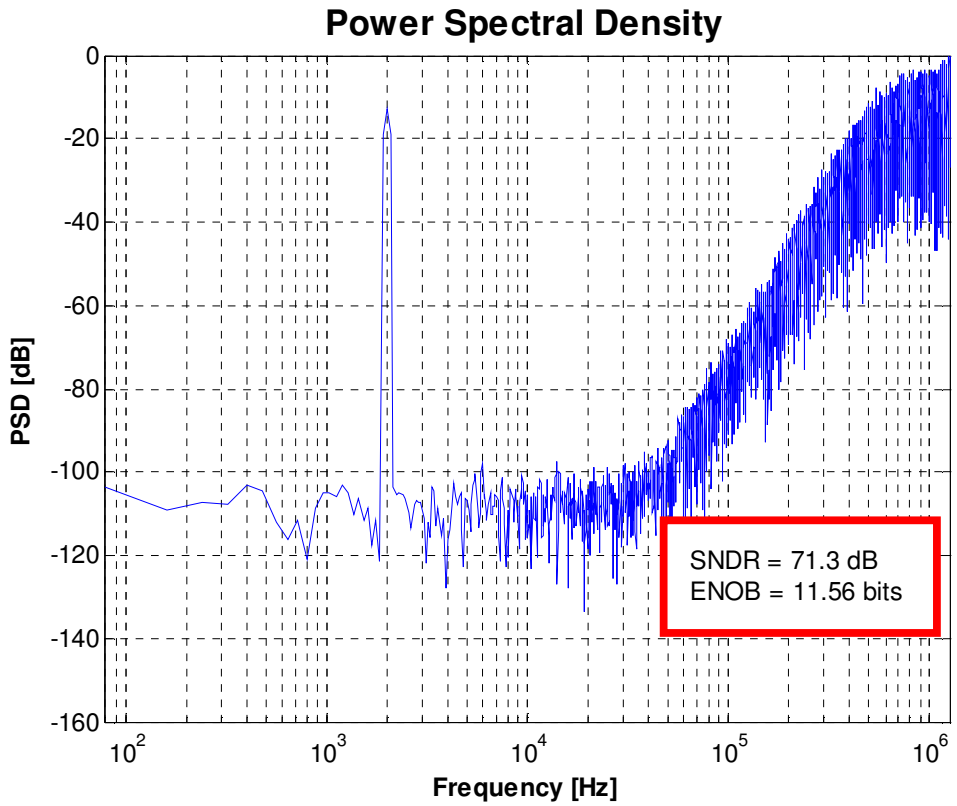


Fig. 6.4: Simulink spectrum of the 4th-order MASH

B. Circuit Level Design

The circuit-level innovations in the dissertation have been elaborated in Chapter V. In this section, additional circuit blocks and implementation details will be discussed. Hspice simulations have been conducted to demonstrate the circuit concepts.

1. Second-order modulator

Fig. 6.5 shows the circuit diagram of the super inverter-based 2nd-order modulator and the associated timing arrangements. Fig. 6.6 – 6.7 show the transient responses at different internal nodes of the modulator. Due to the use of floating sampling, the input/output common-mode levels of the inverters are kept at the mid-rail over time. In addition, the inverters settle quickly after each transition. The modulator output clearly shows the delta-sigma characteristic, also shown in Fig. 6.8.

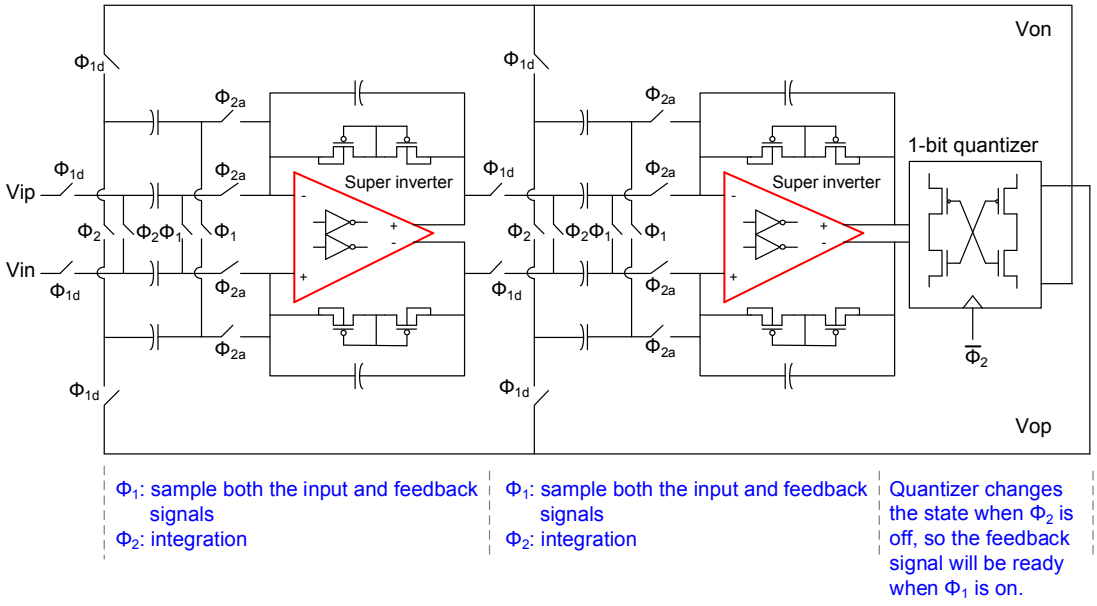


Fig. 6.5: Circuit diagram of the prototyped 2nd-order modulator

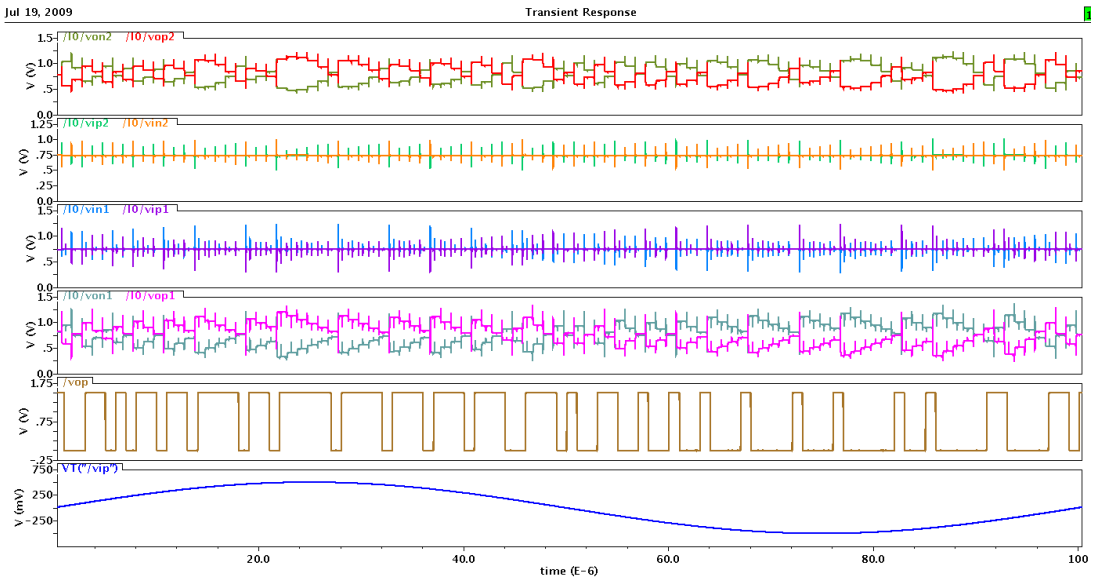


Fig. 6.6: Transient responses of the modulator

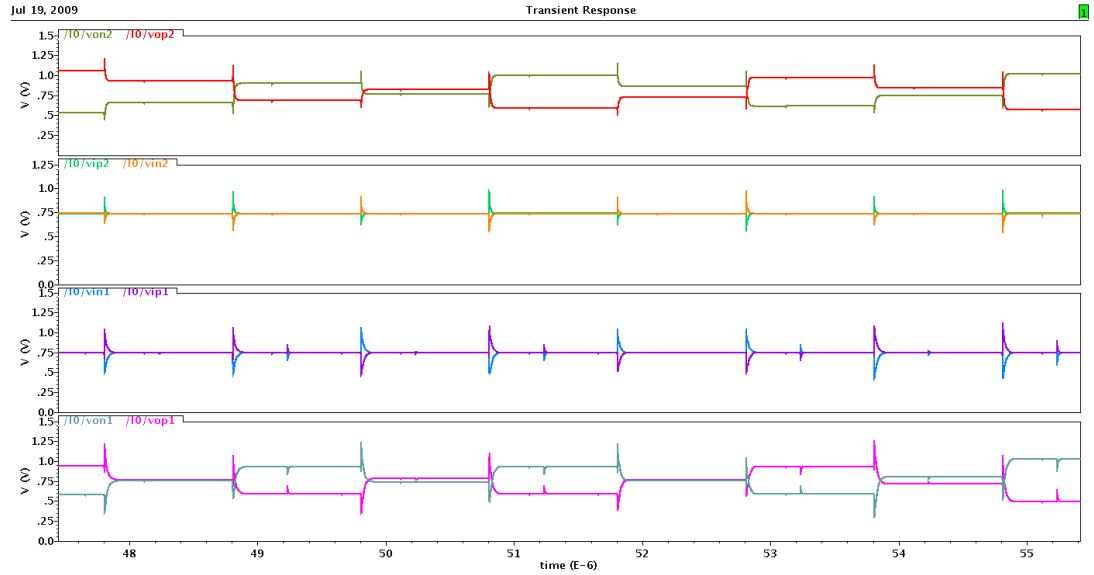


Fig. 6.7: Zoom-in view of the waveforms

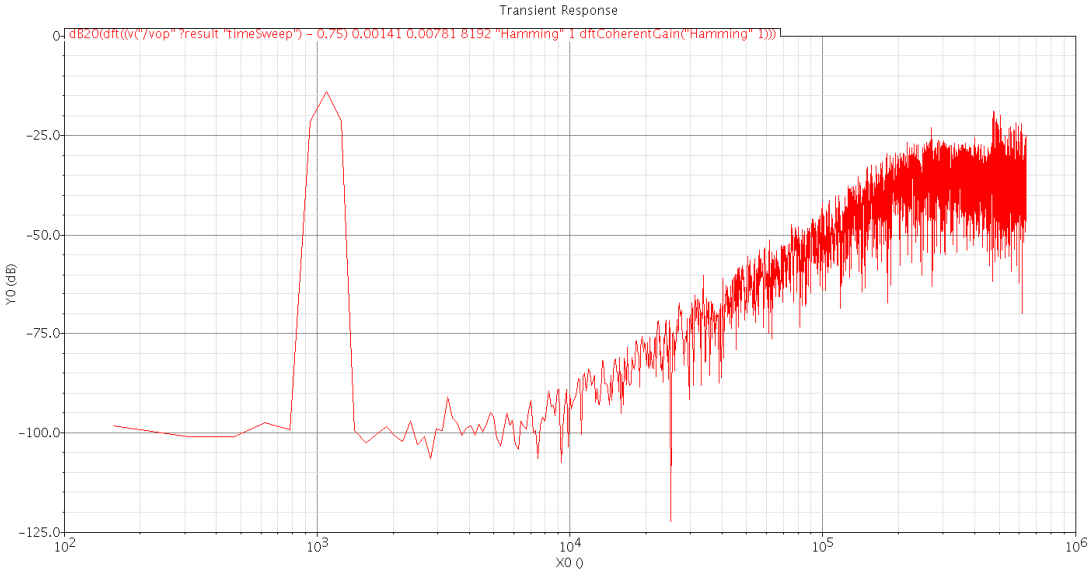


Fig. 6.8: Simulated output spectrum based on an 8192-point DFT

2. Pseudo-resistor

Pseudo-resistors are employed in the modulator design to setup the input DC conditions for the inverter amplifiers and provide necessary CMFB function. A PMOS device can be used to form a MOS diode (blue) and a BJT diode (red) in anti-parallel direction [Otis07]. If the DC voltage across the device is less than the turn-on voltage of the diodes, the leakage current will be so small that very high resistance can be realized with negligible chip area.

To increase the voltage range, two PMOS devices can be reversely-connected, as shown in Fig. 6.9. When V_1 is greater than V_2, the leakage current goes through the MOS diode of M_1 and the BJT diode of M_2, and vice versa. Since two diodes are in

series in the DC path, higher voltage is required to draw the same level of current. Fig. 6.10 shows the simulated resistance of the pseudo-resistor as the differential voltage is swept from -1 V to 1V. Since the output swings of the SC integrators are limited in a range through the feedback, the pseudo-resistors mostly operate in the high-resistance region. During the chip power-on, the large voltage drop would actually turn on the diodes and large charging current results, greatly assisting with the amplifier startup.

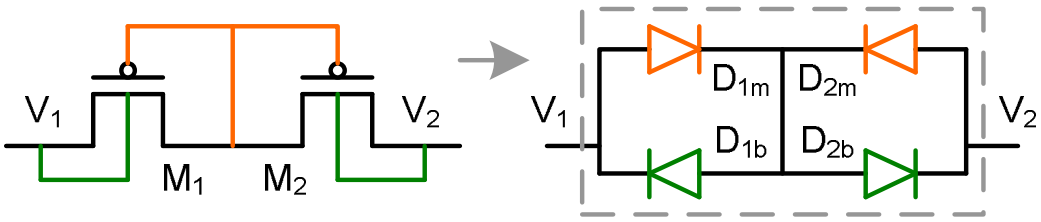


Fig. 6.9: Pseudo-resistor and its circuit representation

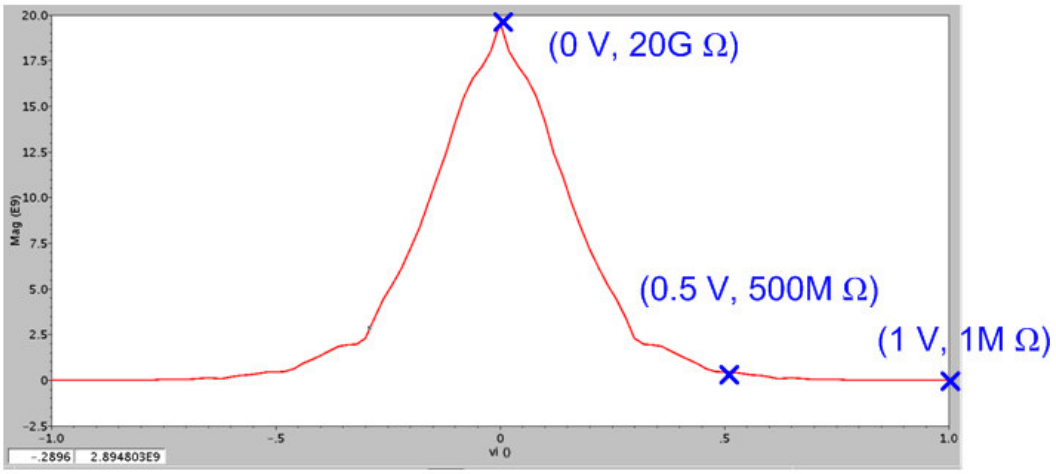


Fig. 6.10: Simulated resistance of the pseudo-resistor

3. Quantizer

Fig. 6.11 shows the circuit diagram of the single-bit quantizer employed in the modulator design. A fully-differential Bazes amplifier serves as the pre-amplifier to enhance the sensitivity of the quantizer and isolate the kickback noise from the comparator [Liu01]. The comparator is formed based on a pair of cross-coupled inverters [Montanaro96]. Due to the use of feedback, this latched comparator is much faster than open-loop comparators in generating rail-to-rail swings. The shorting device (M_s) provides a DC-leakage path from either its drain or source nodes to ground. This is used to prevent the leakage-induced output changes after the comparator has made a logic transition. The outputs of the comparator are fed into a NAND-based RS latch. During the reset phase of the comparator, the RS latch can hold the current output states till the next comparison. For the testing purpose, two big inverters are employed for buffering the digital outputs.

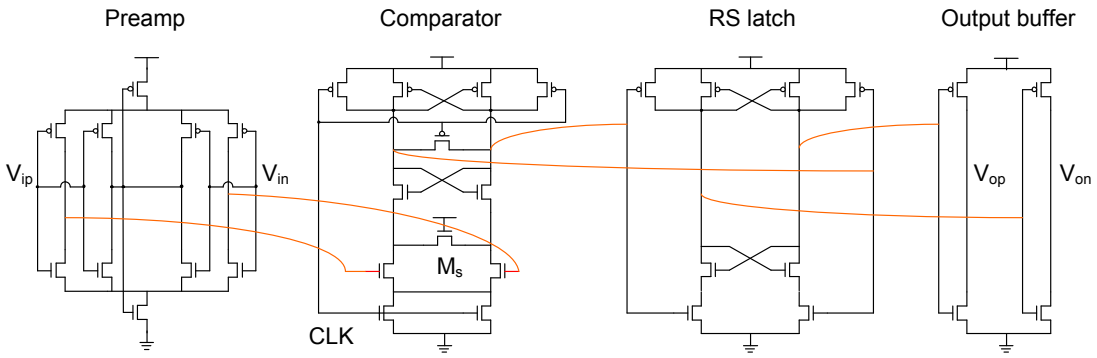


Fig. 6.11: Circuit diagram of the single-bit quantizer

4. Clock generator

Fig. 6.11 shows the circuit diagram of the non-overlapping clock generator. A pair of cross-coupled NAND or NOR gates can be utilized to generate two non-overlapping clock signals from the input [Martin87]. Delay cells, formed by a series of transmission gates, are used to adjust the gap between the on-phases of the two output clocks. Aside from the transmission-gate method, current-starved inverter cells can also do the same job. By pumping small DC current into the inverters, large time constants can be realized, and this may be more suitable for low frequency applications. In the circuit, a NAND gate generates a delayed falling edge for Φ_1, and a NOR gate generates an advanced rising edge for Φ_2. Finally, scaled buffer chains are employed to align the reverse clock phases and drive the capacitive loadings.

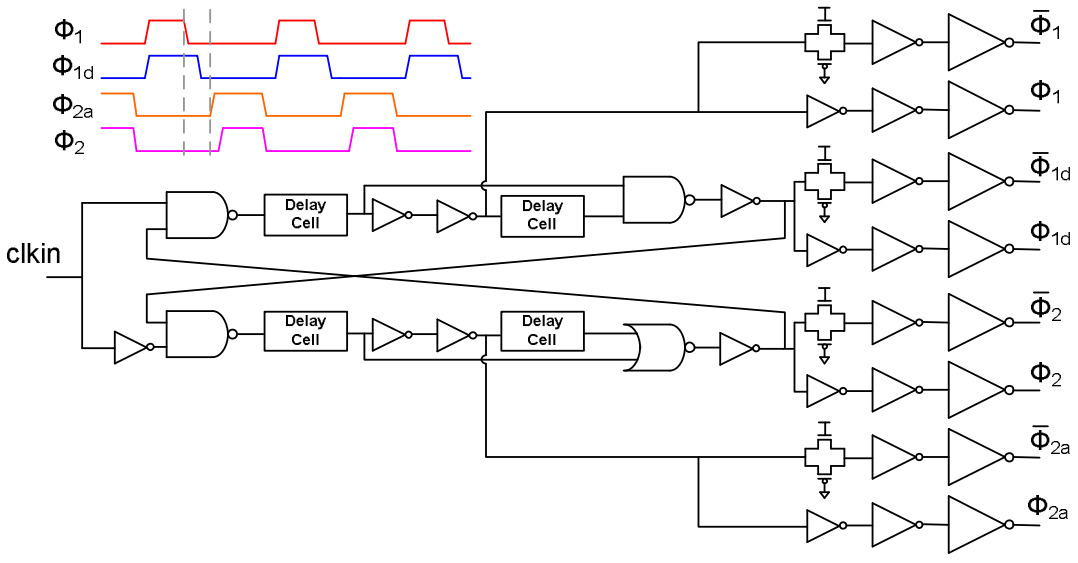


Fig. 6.12: Circuit diagram of the non-overlapping clock generator

5. MASH architectures

Several 4th-order MASH architectures have been prototyped based on the inverter amplifiers. For comparison purposes, a MASH prototype without the CDS circuit is included, as shown in Fig. 6.13. The timing arrangements are explained in the figure. At the first integrator, two sampling circuits have been combined to reduce the KT/C noise in the prototypes since the two signal paths have the same gain factor. Both stages of the 2nd order modulator utilize the Boser-Wooley structure.

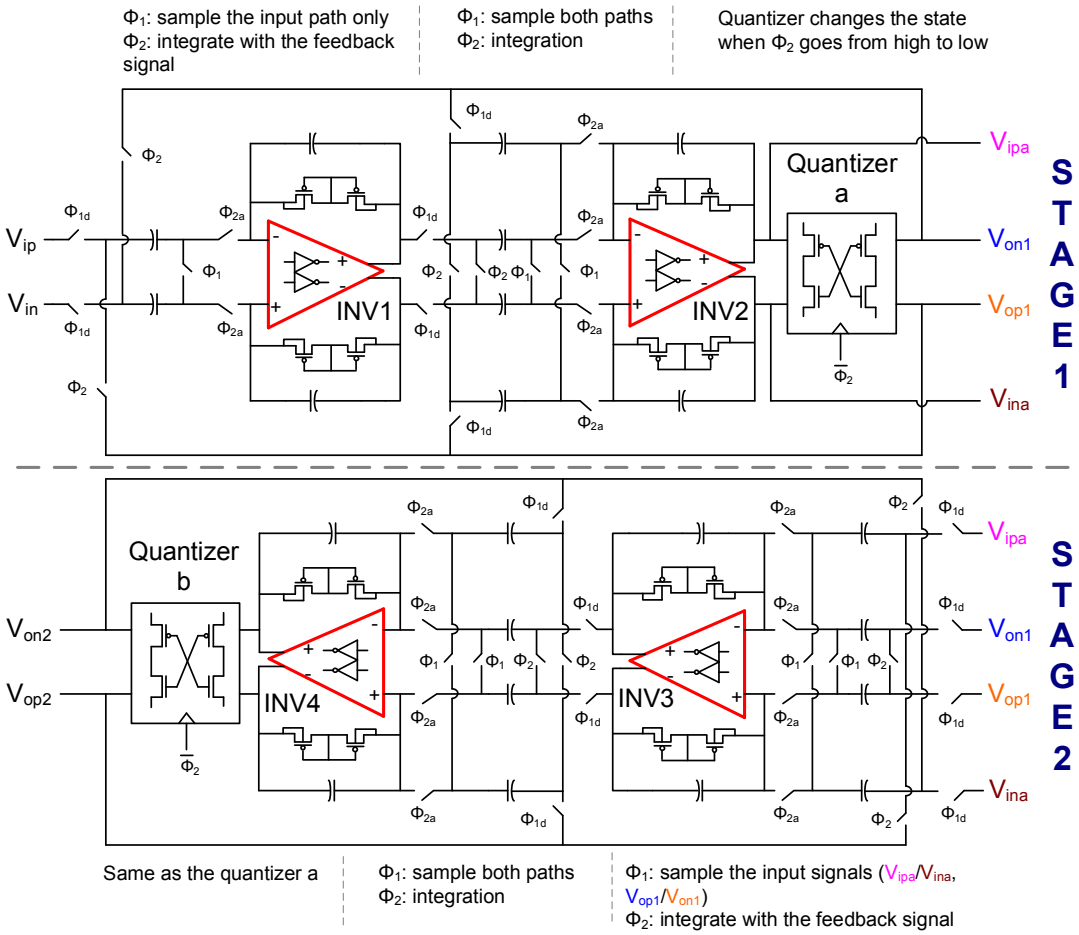


Fig. 6.13: Circuit diagram of the 4th-order MASH architecture (no CDS)

Fig. 6.14 illustrates the MASH architecture with the CDS circuit employed in the first integrator, which is the most critical component for the overall loop filter. This is arranged to reduce the system complexity but also take advantage of the CDS improvements. For the same reason, the first amplifier needs to attain better performance than the other amplifiers, and the loop filter is optimized for higher power efficiency.

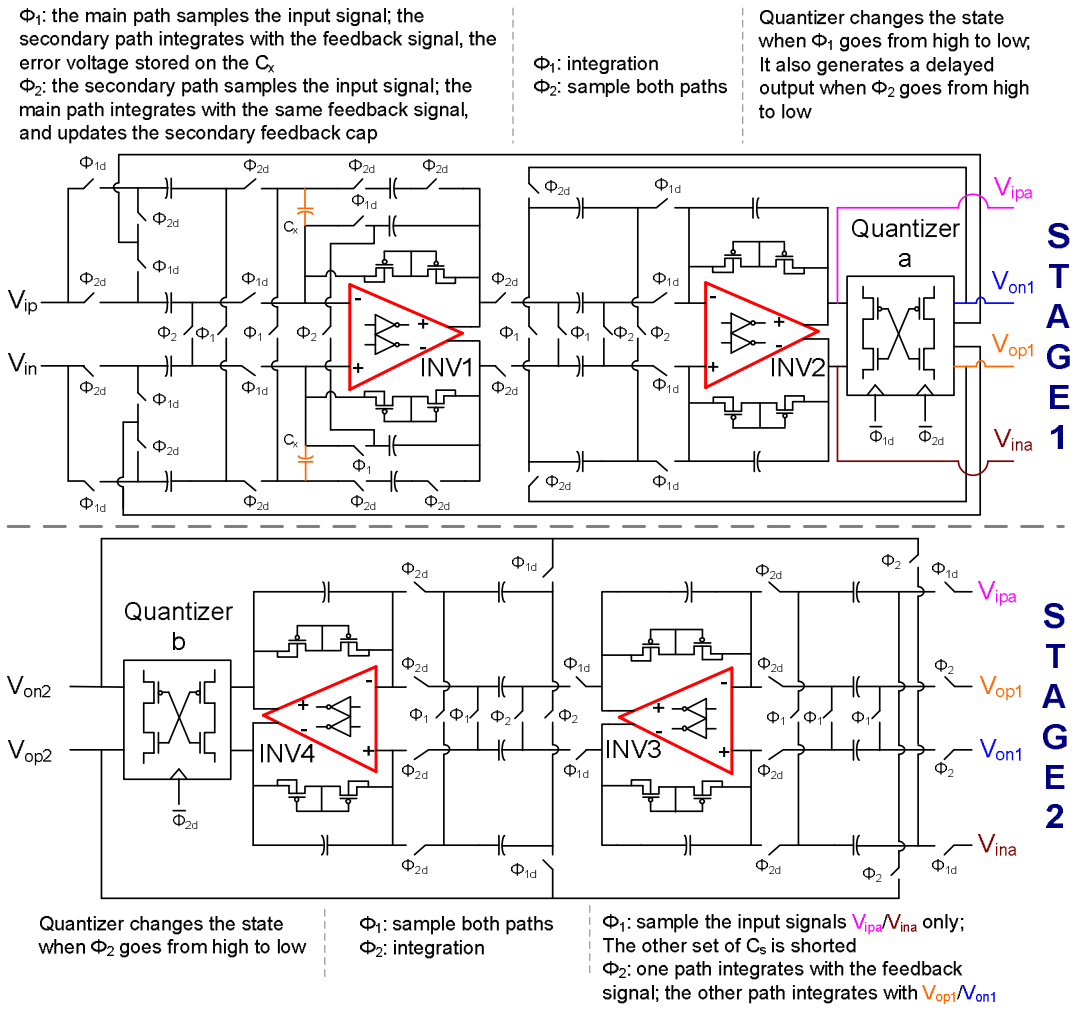


Fig. 6.14: Circuit diagram of the 4th-order MASH architecture (CDS included)

After including the CDS circuit, the timing arrangements becomes more complex. Since the main path at the first integrator needs to feed into the second integrator in the integration phase, the clocks for the second integrator need to be swapped: it samples in Φ_2 and integrates in Φ_1. Hence, the quantizer generates the output as soon as Φ_1 is off, and the new output will be available for the next Φ_2. For the main path and secondary path at the first integrator to see the same feedback signal, the output needs to be further delayed for half clock cycle. Therefore, the quantizer also needs to latch the output for a whole clock cycle when Φ_2 is off, and this delayed output feeds to the input of the first integrator. Fig. 6.15 illustrates the timing diagram of the first stage: the input signal (X_1) and feedback signal (Y_d) to the first integrator; the input signal (X_2) and feedback signal (Y) to the second integrator.

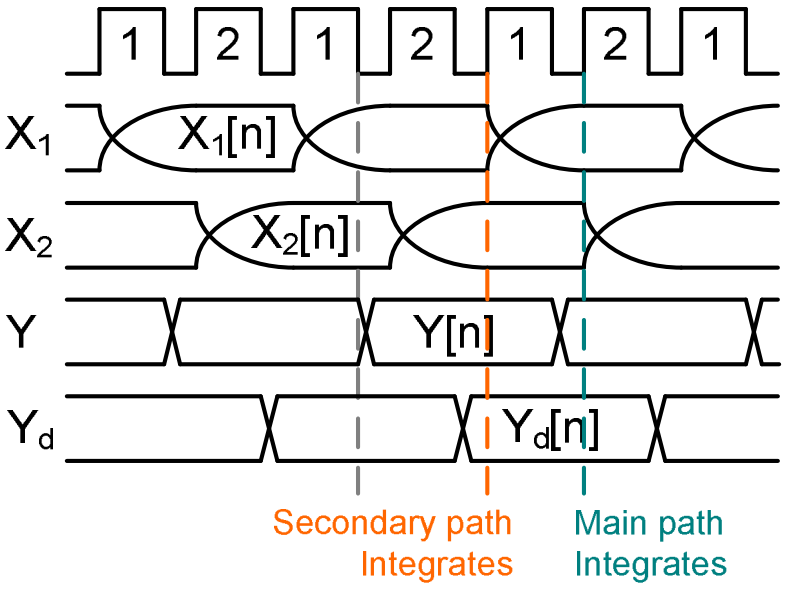


Fig. 6.15: Timing diagram of the first modulator stage

Table 6.3 summarizes the configurations of the different MASH prototypes in the dissertation. MASH1 uses the high-gain inverter amplifiers, so no CDS circuit is included. MASH2 utilizes the super inverter with no CDS for comparison. MASH3 employs the super inverter amplifiers which have been arbitrarily sized for ultra low power consumption. MASH4 has the CDS circuit and optimally-sized super inverter amplifiers. The measurement results of these prototypes will be compared in the next chapter.

Table 6.3: Configurations of the 2-2 MASH prototypes

	Amplifier structure	CDS
MASH1	High-gain inverter (at the first integrator); new inverter (at the rest integrators)	No
MASH2	Super inverter (at all the integrators)	No
MASH3	Ultra low current super inverter (at all the integrators)	Yes
MASH4	Super inverter (at all the integrators)	Yes

C. Mask Layout Design

In this section, the general considerations and hierarchical views of the mask layout will be discussed. Good layout practices strongly affect the actual performance of the fabricated circuits, so it is important to understand the implications and limitations in the layout. Through careful floor-planning of the layout, the chips achieve very small form factor.

1. General considerations

The layouts of the 2^{nd} order modulator and 4^{th} order MASH prototypes were conducted in Cadence Virtuoso with the following guidelines:

A. The layout should be fully symmetrical at all levels. This is important to minimize even-order harmonic distortion and the overall size.

B. The lower level cells will be laid out and verified first, which can then be reused for higher level layouts. This makes the layout design more manageable.

C. At the cell level, all the PMOS or NMOS devices should be put together, and the gate ordering can be optimized using Euler Path approach [Roy07]. This makes a more compact layout, reducing the parasitics and signal coupling.

D. Dummy gates are used at the foremost sides of the cell layouts to create a uniform ambient environment for all gate fingers.

E. Double guard rings are utilized at the block level to reduce substrate noise.

F. The clock generator and digital buffers should be far away from the analog circuitry, minimizing the switching noises from digital circuits.

G. On-chip bypass capacitors should be tied to the supplies as much as possible.

2. Layout views

Fig. 6.16 shows the layout view of the 2nd-order modulator in a 130 nm CMOS process. It occupies a silicon chip area of 135 µm by 218 µm. Fig. 6.17 shows the layout view of the 4th order MASH prototypes. It shows the prototype MASH1, MASH2, MASH3, and MASH4 from left to right, and each prototype occupies roughly 150 µm by 400 µm chip area.

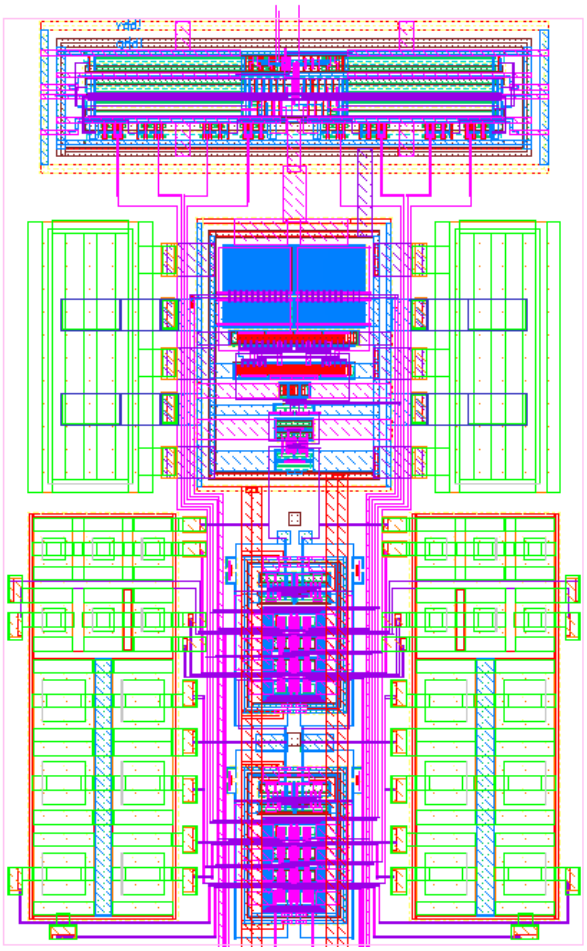


Fig. 6.16: Layout view of the 2nd-order modulator (135 µm x 218 µm)

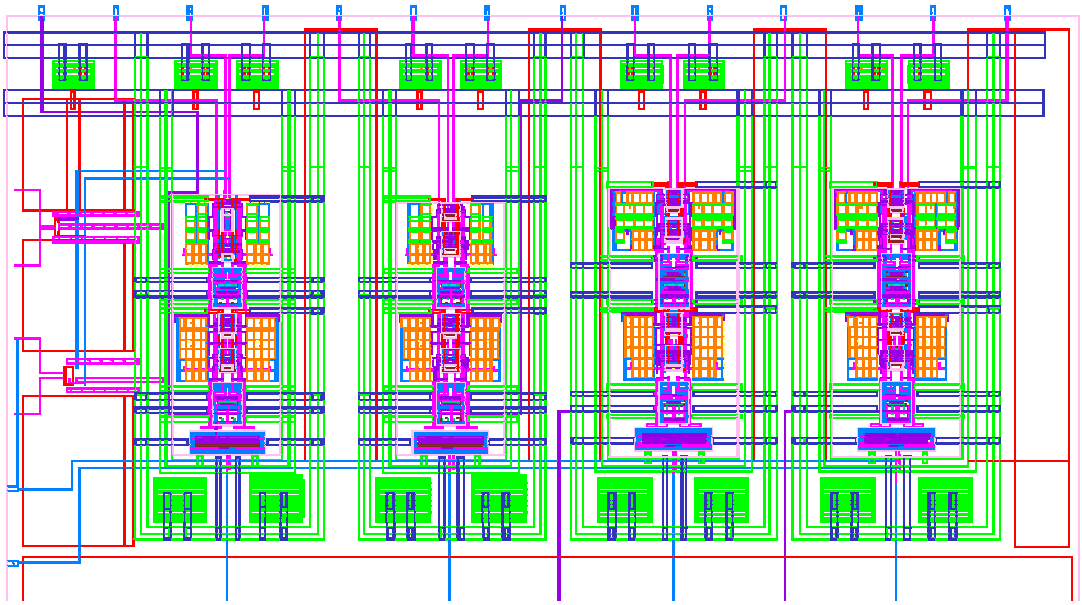


Fig. 6.17: Layout view of the MASH prototypes

VI. CHIP MEASUREMENT

A. Test Environment Setup

Fig. 7.1 shows the assembled testing board and equipments for the measurement of the 2nd-order modulator. The testing board uses a two-layer process, and contains the decoupling capacitors and various kinds of connectors. For the measurement of the MASH prototypes, the board has more testing ports but still follows the same design methodology. It will not be discussed here for simplicity. Due to the use of self-biasing inverters, all the ADC chips require relatively simple testing boards.

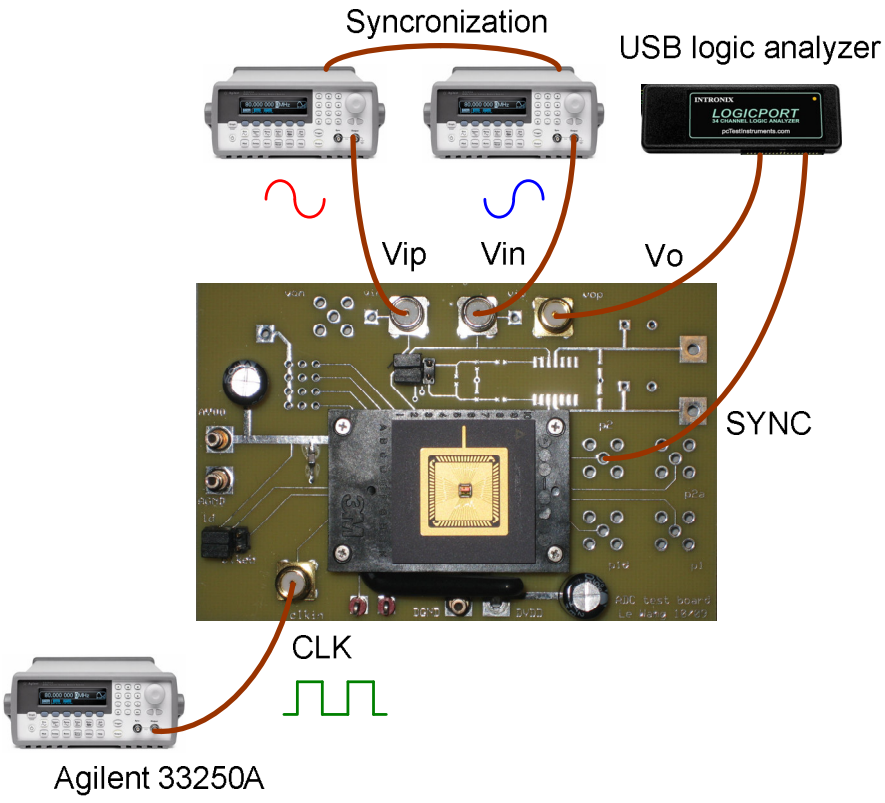


Fig. 7.1: Testing board and the equipment setup

Two function generators (Agilent 33250A) are synchronized to generate the differential inputs for the modulator. After synchronization, the relative phase can be adjusted to make these two signals differential. One problem with this method is that the relative phase needs to be readjusted whenever the frequency is changed. There are also other methods for generating differential signals. Some audio transformers from Tamura can handle signal frequencies less than 10 KHz, but the transformer might not be good to drive switched-capacitor inputs. NI cards can also be programmed with the aid of Labview to produce the waveforms.

Another 33250A is also used to generate the clock input. For a 1.6 MHz clock signal, the equipment has roughly 600 ps (RMS) clock jitter according to the data sheet [Agilent09]. Eq. 3.30 shows the maximum SNR of an ADC due to clock jitter. For a 5 KHz signal and 100 OSR, Eq. 7.1 calculates the maximum SNR, which is much greater than the target SNR. Therefore, the clock jitter from the equipment would not limit the chip performance.

$$SNR_{\max} = -19 + 20\log_{10}\left(\frac{200\mu}{600p}\sqrt{100}\right) = 105 \text{ (dB)} \qquad (7.1)$$

The output binary bits are latched into a USB logic analyzer for post-processing in Matlab. The one shown in Fig. 7.1 (Intronix LA1034) has a buffer depth of only 2048 points. To store more than 32K binary bits, advanced logic analyzers, such as GWINSTEK GLA-1016, need to be used. In all the following characterizations, the low frequency bound is set at the third FFT bin (=3×F_s/32000).

B. Measurement results

1. Second-order modulator

Fig. 7.2 shows the chip microphotograph of the 2nd-order modulator. A measured output spectrum, clocked at 1.6 MHz, is shown in Fig. 7.3. The 32K-point DFT with a hanning window has been employed to plot the spectrum. No offset-cancellation mechanism is included in this prototype, and this accounts for the -40 dBFS DC tone in the spectrum. Fig. 7.4 plots the measured SNR and SNDR over the 8 KHz of neural signal bandwidth versus the input amplitude. At 1.5 V power supply, the peak SNR and SNDR of the modulator are 66 dB and 62 dB, respectively.

The supply noise rejection is measured by coupling a -20 dBFS 2 KHz noise tone onto the supply while keeping the inputs shorted. Due to the fully differential nature of the super inverter, the modulator achieves 60 dB power supply rejection ratio (PSRR), as illustrated in Fig. 7.5. Fig. 7.6 shows the measured peak SNR and SNDR versus supply voltage. The roll-off of the SNDR is due to the nonlinear distortion of the inverter amplifier at low voltage supply.

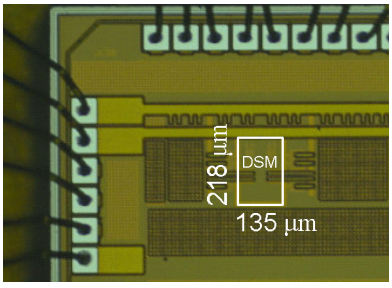


Fig. 7.2: Chip microphotograph of the 2nd-order modulator

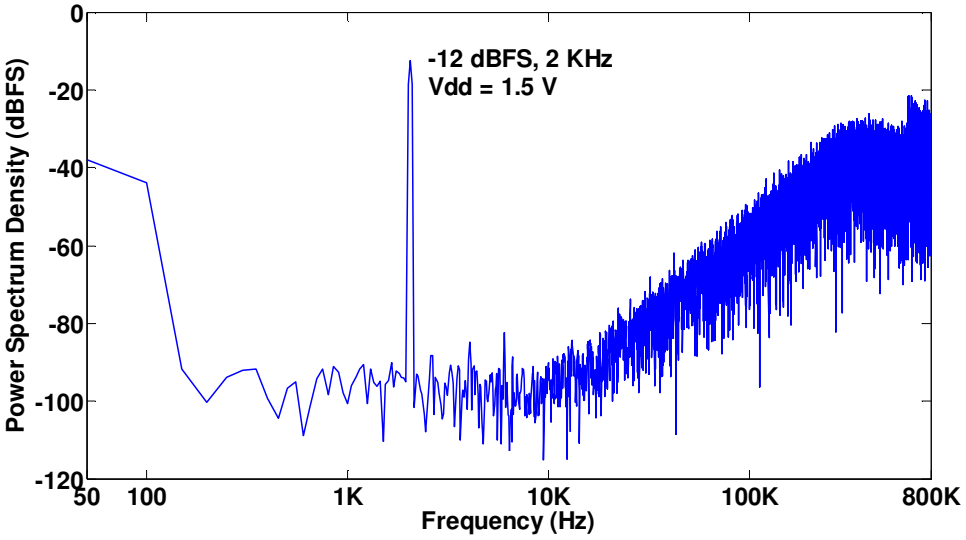


Fig. 7.3: Measured output spectrum of the 2nd-order modulator

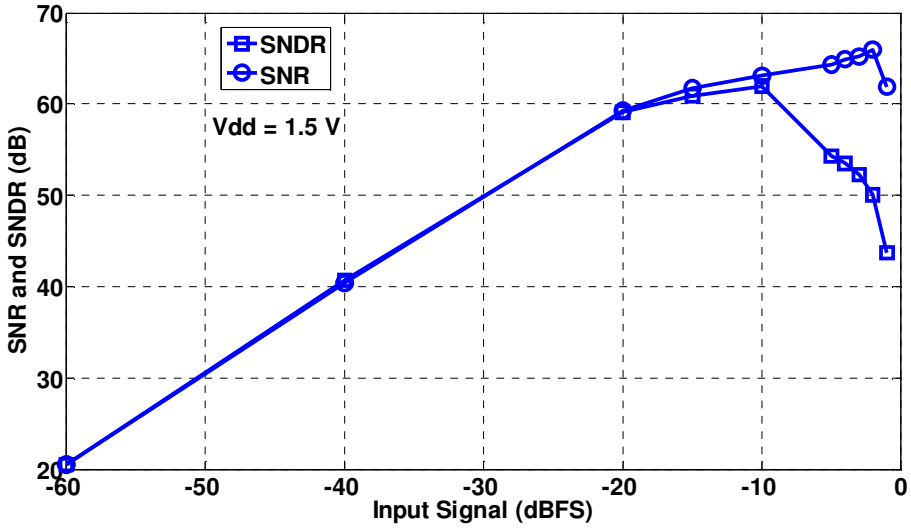


Fig. 7.4: Measured SNR/SNDR curve of the 2nd-order modulator

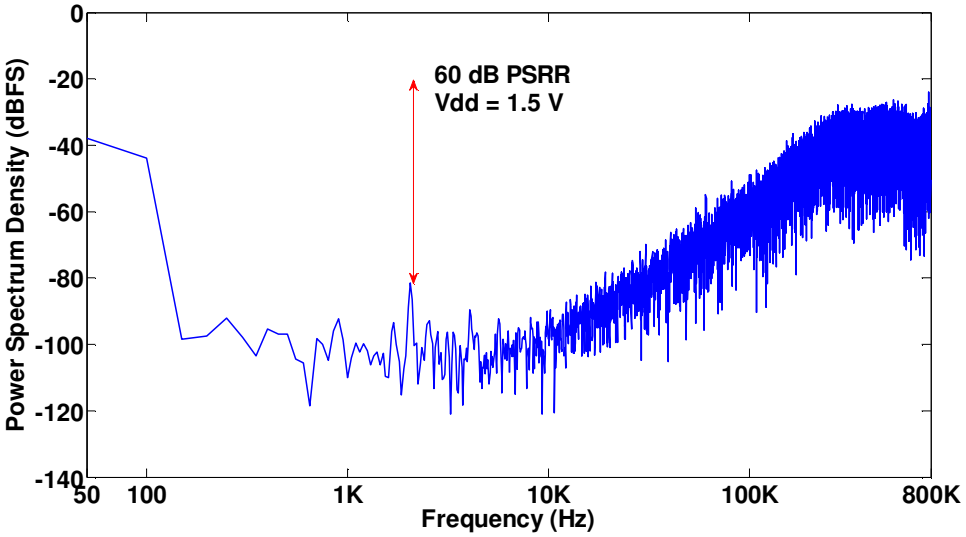


Fig. 7.5: Measured PSRR with -20 dBFS 2 KHz supply noise

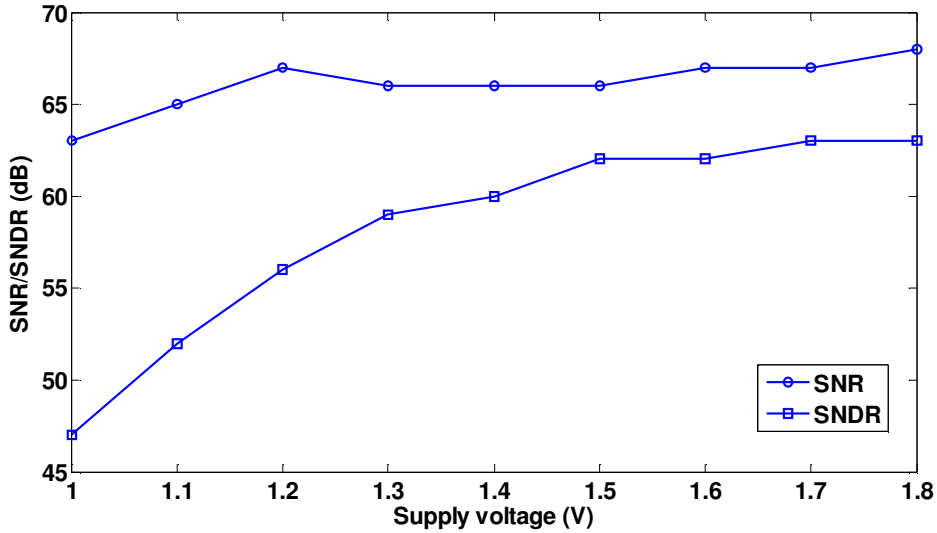


Fig. 7.6: Peak SNR and SNDR versus supply voltage

The measurement results at both 1.5 V and 1.2 V power supplies are summarized in Table 7.1, with the figure of merit (FOM) defined as in Eq. 7.1. A performance comparison of several recently published SC delta-sigma modulators is given in Table

7.2. Due to the use of the self-biased super inverter, this modulator achieves an excellent performance in the power efficiency and PSRR, enabling a high FOM.

$$FOM = \frac{Power}{2 * BW * 2^{(DR-1.76)/6.02}} \tag{7.1}$$

TABLE 7.1: Measurement summary for the modulator

Supply Voltage	1.5 V	1.2 V
Sampling Frequency	1.6 MHz	
Signal Bandwidth	8 KHz	
Dynamic Range	67 dB	68 dB
Peak SNR @2 KHz	66 dB	67 dB
Peak SNDR @2 KHz	62 dB	56 dB
PSRR	60 dB	
SFDR	70 dB	
Power Consumption in the core*	20 µW	4.8 µW
Total Power Consumption	27 µW	6.5 µW
FOM (pJ/conversion-step)	0.7	0.14
Chip Area/Process	0.03 mm^2/0.13 µm CMOS	

* Excluding power consumption in clock generator and output buffers

Table 3.2: Performance comparison

Reference / Technology	BW	Dynamic Range	PSRR	Power	FOM (pJ/step)
[Han09] */ 0.35 µm	8 KHz	76 dB	37 dB	5.6 µW	0.07
[Van08] / 65 nm	200 KHz	77 dB	N/A	950 µW	0.41
[Wooley08] / 0.18 µm	25 KHz	100 dB	N/A	870 µW	0.21
[Goes06] / 0.18 µm	10 KHz	83 dB	N/A	200 µW	0.86
[Wang10] / 0.13 µm	8 KHz	68 dB	60 dB	4.8 µW	0.14

* Modulator-II in [Han09] is used for comparison

2. MASH prototypes

The 4th-order MASH prototypes have been fabricated in the same CMOS process, and Fig. 7.7 shows the quadrant chip microphotograph. Each prototype occupies a chip area of roughly 0.06 mm^2. All the four prototypes are connected to the same power supplies. For minimizing the supply noise, additional control signals are provided to turn off the clock block of a prototype when it is not under test. The testing setup is similar as the 2nd order prototype, and the digital cancellation was performed in Matlab using an ideal gain of 6 (see Appendix A).

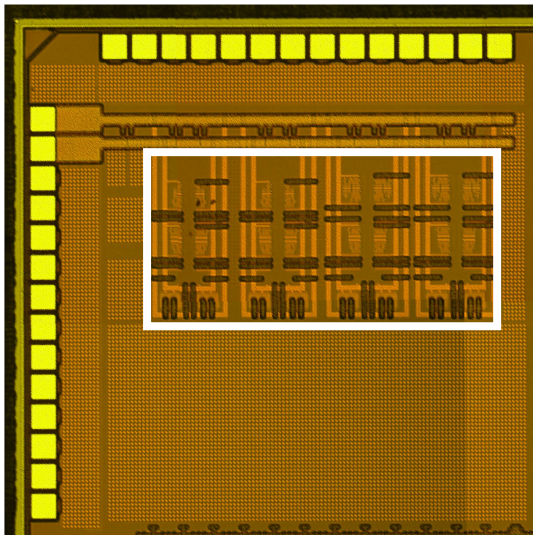


Fig. 7.7: Chip microphotograph of the MASH prototypes

MASH1: It uses the high-gain inverter amplifier at the first integrator, with no CDS circuit included. The other integrators employ the low power and low gain inverter amplifiers. Fig. 7.8 shows the measured output spectrums of the prototype MASH1, clocked at 2.56 MHz. Clearly, a 4th-order noise shaping is achieved, as shown in the red curve. Due to the use of the high-gain amplifier, the amplifier

nonlinearity limitation is mitigated, and the in-band noise floor becomes roughly 10 dB lower than the 2nd-order modulator shown in Fig. 7.3.

The 2nd-order delta-sigma output spectrum from the first stage is also shown, which almost overlaps the 4th-order spectrum from DC to 10 KHz. At 10 KHz, the 2nd order noise spectrum starts rising at a rate of 40 dB per decade, but the 4th order spectrum slowly changes from 10 KHz to 100 KHz. Hence, the MASH architecture may be more suitable for wide bandwidth applications, and bigger input capacitors are necessary for achieving higher resolution.

Fig. 7.9 shows the measured 4th-order SNR and SNDR over the 10 KHz bandwidth versus the input amplitude. At 1.5 V power supply, the peak SNR and SNDR of the MASH1 are 76.5 dB and 72.6 dB, respectively. Table 3.3 summarizes the results for MASH1, with the FOM redefined in Eq. 7.2.

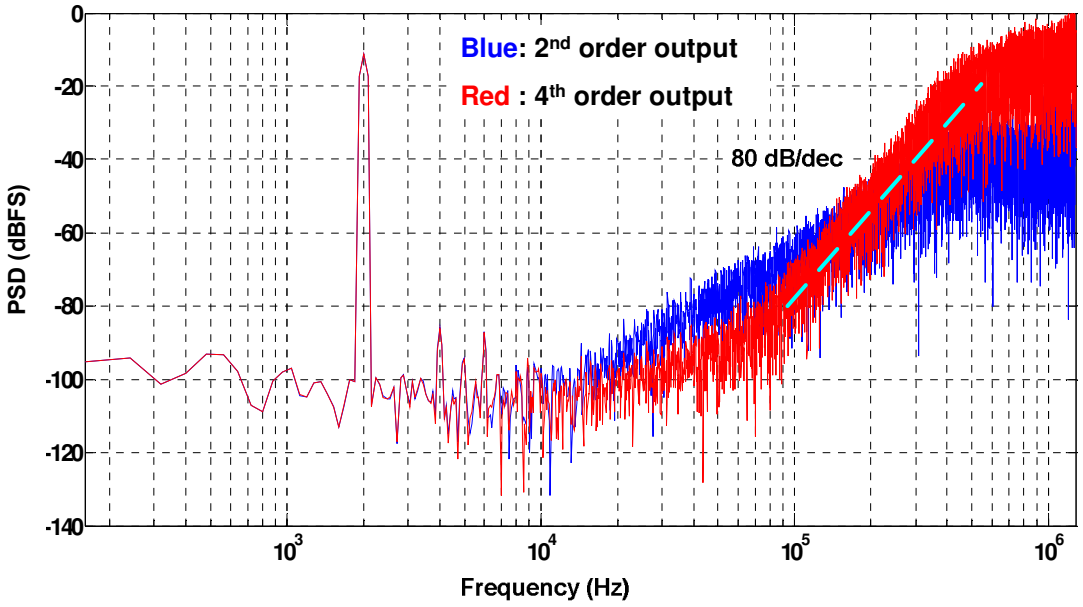


Fig. 7.8: Measured output spectrums of the prototype MASH1

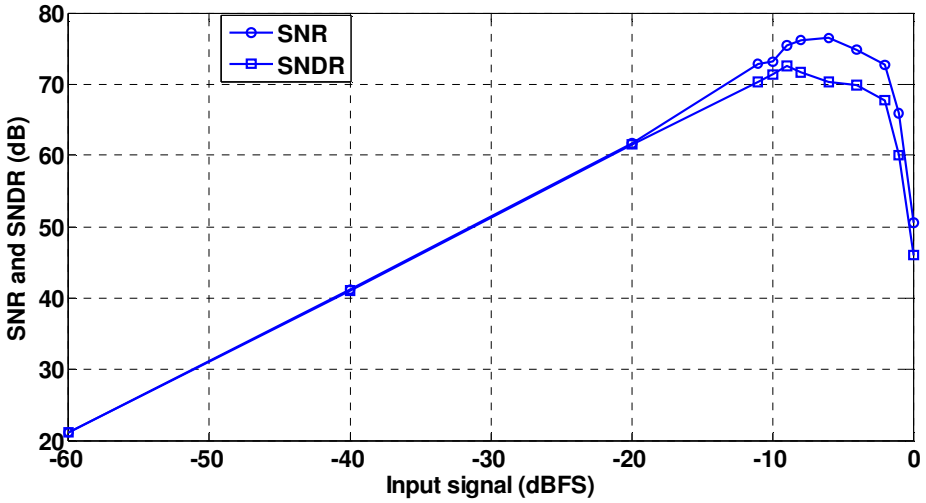


Fig. 7.9: Measured SNR/SNDR curve of the prototype MASH1

$$FOM = \frac{Core\_Power}{2 * BW * 2^{(SNDR-1.76)/6.02}} \tag{7.2}$$

TABLE 7.3: Measurement summary for MASH1

Supply Voltage	1.5 V
Sampling Frequency	2.56 MHz
Signal Bandwidth	10 KHz
Dynamic Range	82.5 dB
Peak SNR @2 KHz	76.5 dB
Peak SNDR @2 KHz	72.6 dB
SFDR	75 dB
Power Consumption in the core*	28 µW
Total Power Consumption	35 µW
FOM (pJ/conversion-step)	0.4
Chip Area/Process	0.06 mm^2/ 0.13 µm CMOS

* Excluding power consumption in clock generator and output buffers

MASH4: It uses the optimized super inverter for the whole loop filter, and the floating CDS circuit is added at the first integrator. Fig. 7.10 shows a 4th order delta-sigma spectrum (red curve). Due to the use of the CDS circuit, the in-band noise floor is even 5 dB lower than MASH1. Fig. 7.11 shows the measured 4th-order SNR and SNDR over the 10 KHz bandwidth versus the input amplitude. At 1.5 V power supply, the peak SNR and SNDR of the MASH1 are 77.9 dB and 73.6 dB, respectively. Table 3.3 summarizes the measurement results for MASH4, where the final output is evaluated in a 20 KHz signal bandwidth.

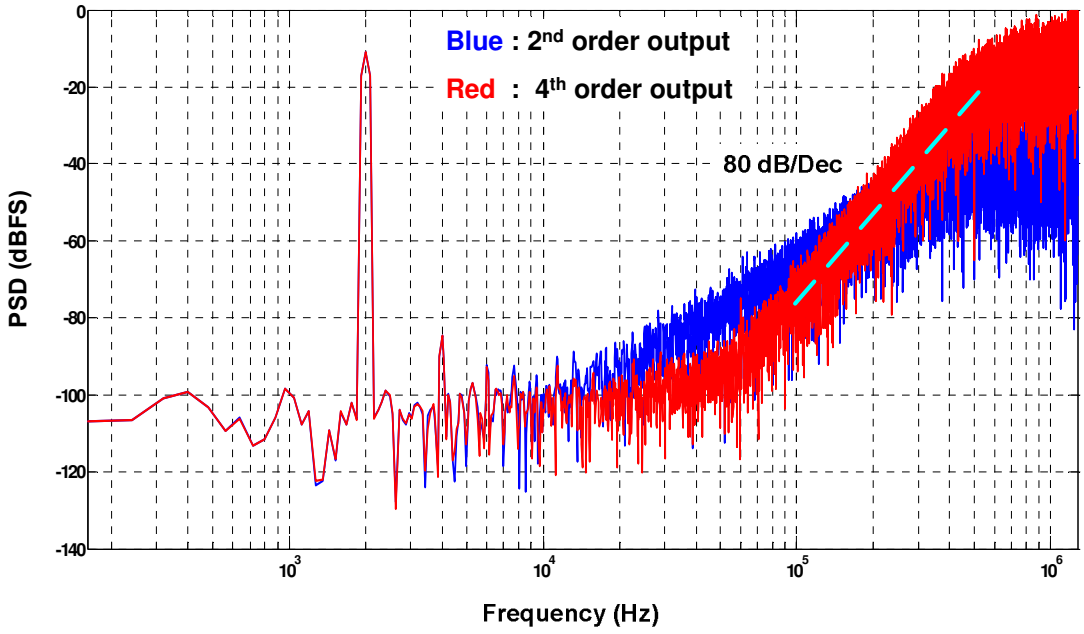


Fig. 7.10: Measured output spectrums of the prototype MASH4

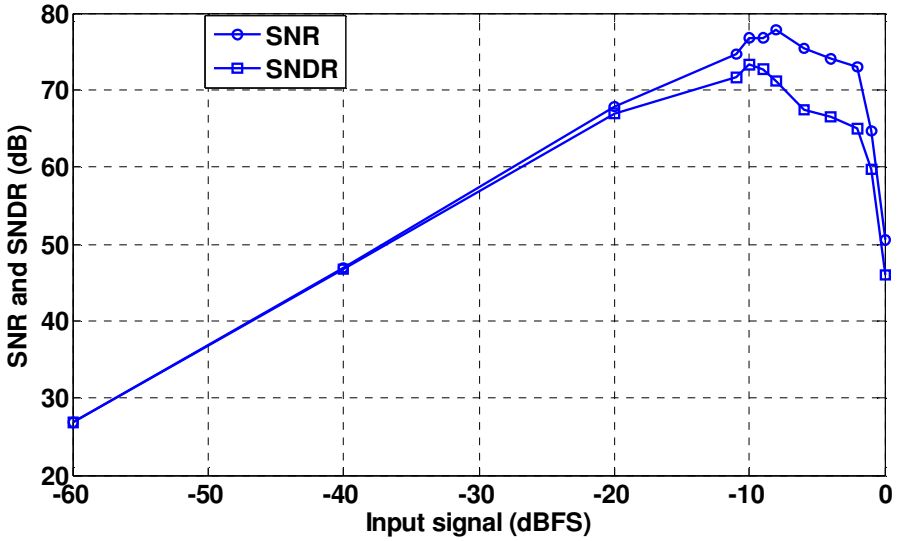


Fig. 7.11: Measured SNR/SNDR curve of the prototype MASH4

TABLE 7.4: Measurement summary for MASH4

Output node	2nd order output	4th order output
Supply voltage	1.5 V	
Clock frequency	2.56 MHz	
Signal bandwidth	10 KHz	20 KHz
Peak SNR	77 dB	73 dB
Peak SNDR	73 dB	71 dB
ENOB	11.8 bits	11.5 bits
Core power consumption	10 µW	18 µW
FOM (pJ/conv.)	0.14	0.15
Die size/Process	0.06 mm^2/0.13 µm CMOS	

MASH4 vs. MASH2: For the comparison purpose, the prototype MASH2 is also evaluated, which uses the same amplifier configuration as MASH4 but excludes the CDS circuit. Fig. 7.12 shows the in-band comparison between these two prototypes by overlaying the 2nd order output spectrums. Due to the use of the CDS circuit, the in-band noise floor of MASH4 is roughly 15 dB lower than MASH2. In addition, the 2nd-order and 3rd-order harmonic distortions of MASH4 are 10 dB and 20 dB lower than MASH1, respectively. Fig. 7.13 shows the out-of-band comparison from the final output spectrums. Since the super inverter is relatively low-gain amplifier, MASH2 does not show 4th-order noise shaping and the noise spectrum levels off from roughly 200 KHz to DC, justifying the gain analysis in the Chapter III.

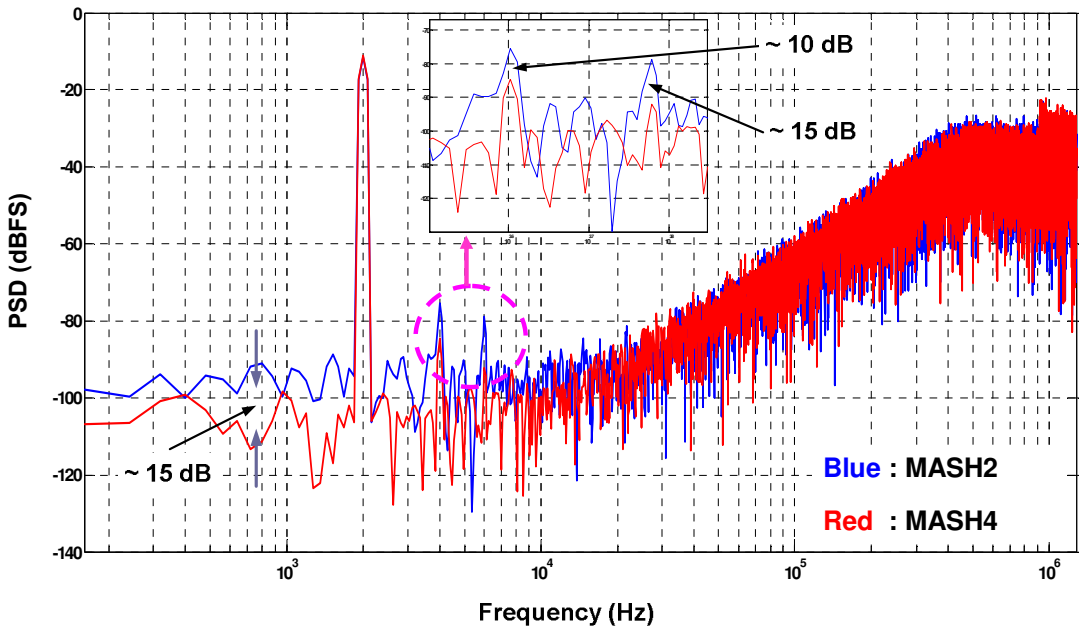


Fig. 7.12: Measured 2nd-order output spectrums of MASH4 versus MASH2

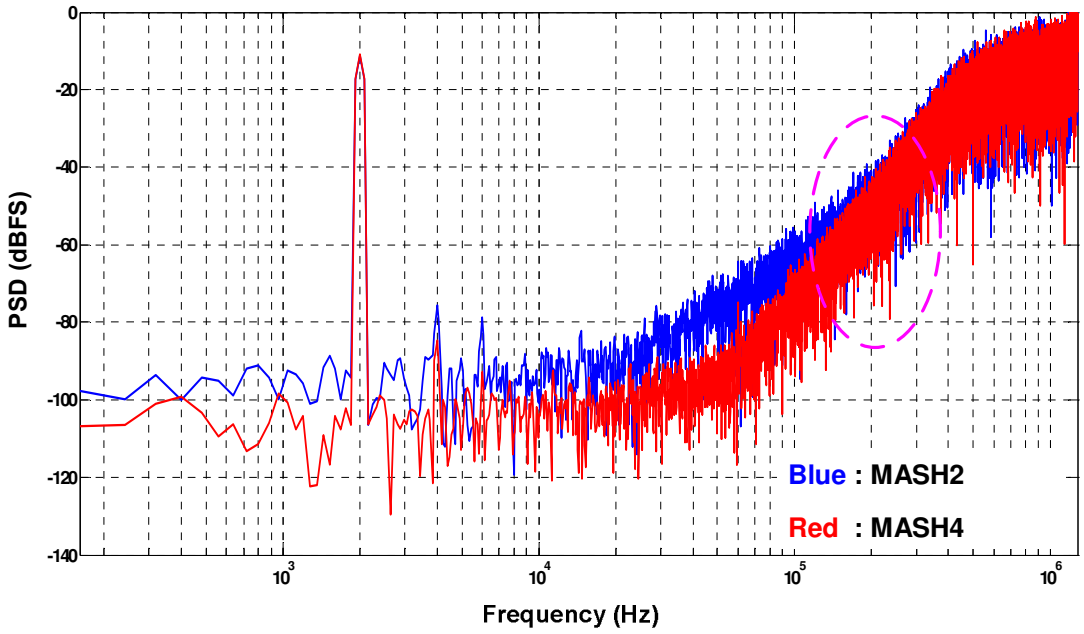


Fig. 7.13: Measured 4th-order output spectrums of MASH4 versus MASH2

MASH4 vs. MASH1: It is also worthwhile to compare MASH4 (the low gain low power super inverter, with CDS circuit) with MASH1 (high gain high power two-stage inverter, no CDS). Fig. 7.14 shows the comparison of the measured 4th order output spectrums. MASH4 attains 1-2 dB lower in-band noise power and 5 dB lower 3rd-order harmonic distortion. Since the CDS circuit is sensitive to the difference between two successive input samples, its performance would degrade as the input amplitude approaches the full-scale. The MASH1 configuration shows slightly better performance for the input amplitude of between -8 to -2 dBFS, as shown in Fig. 7.15. The key characterizations of these two prototypes are compared in Table 7.5.

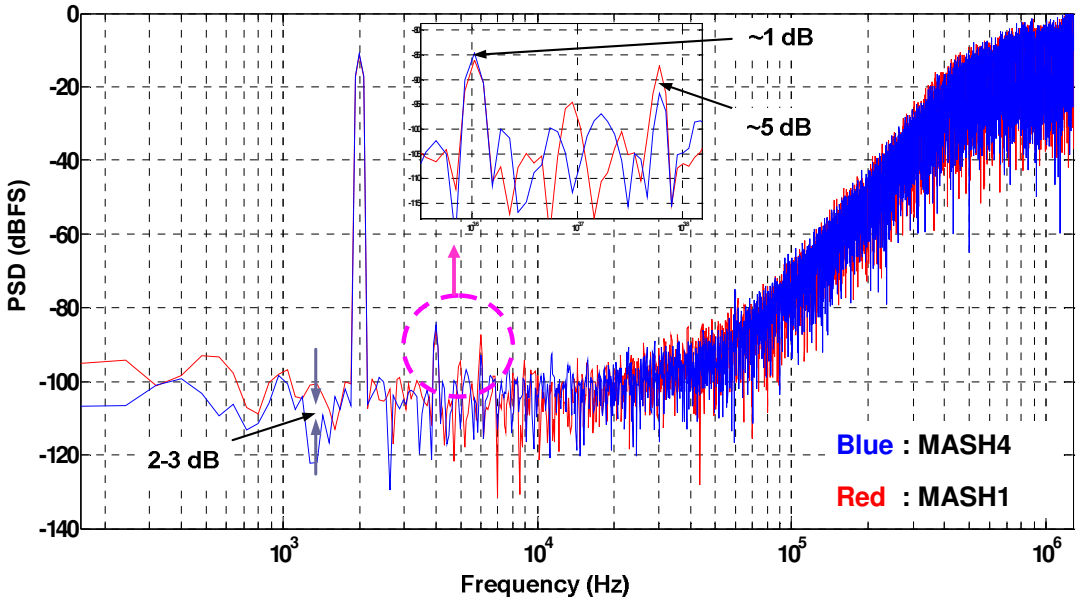


Fig. 7.14: Measured 4th-order output spectrum of MASH4 versus MASH1

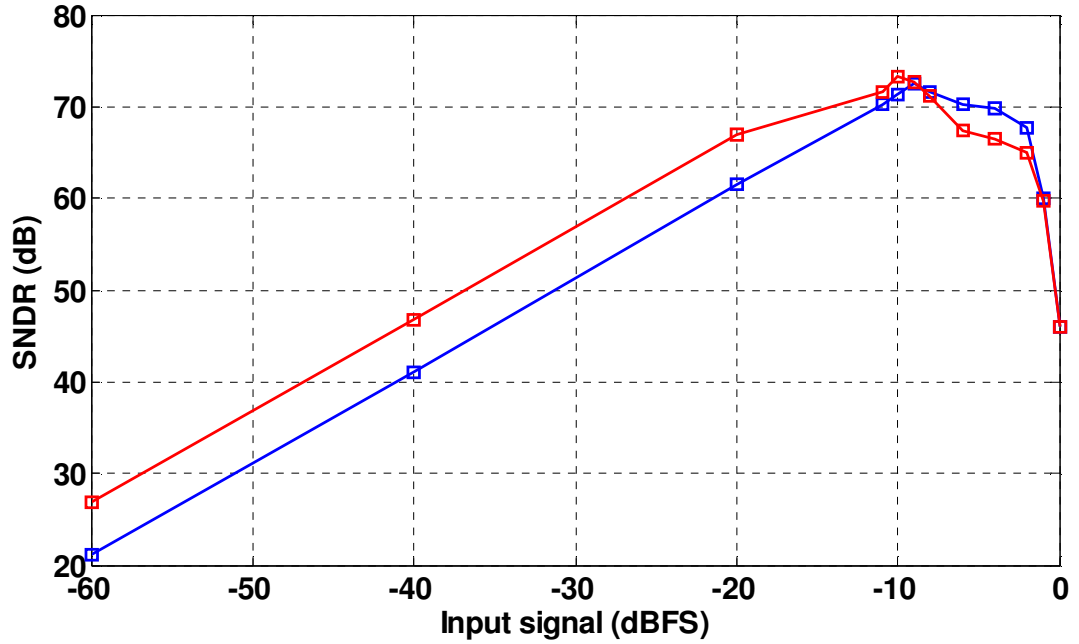


Fig. 7.15: Measured SNDR curve of MASH4 (blue) versus MASH1 (red)

TABLE 7.5: Performance of MASH4 versus MASH1

	MASH4	MASH1
Clock frequency	2.56 MHz	
Signal bandwidth	10 KHz	
Peak SNR	77.9 dB	76.5 dB
Peak SNDR	73.6 dB	72.6 dB
SFDR	75 dB	76 dB
Core power consumption	18 μW	28 μW
FOM (pJ/conv.)	0.27	0.4

MASH3: Its measured outputs do not show reasonable SNR/SNDR, and the in-band noise floor of the plotted spectrum is raised up by several tenth dB. It may be due to the insufficient settling of super inverters using ultra long transistors ($L \geq 2\mu m$).

State of the art: Fig. 7.16 shows the stacking of the reported ADC prototypes in ISSCC from 1997 to 2010. The plot is based on an online ADC survey [Boris10], comparing the energy per conversion (f_s refers to the Nyquist rate) versus the resolution of the ADC. The MASH4 performance (for 20 KH BW) is also overlaid in the figure. The proposed MASH design methodology clearly advanced the state of the art of ADC design in the mid-70 dB SNDR range.

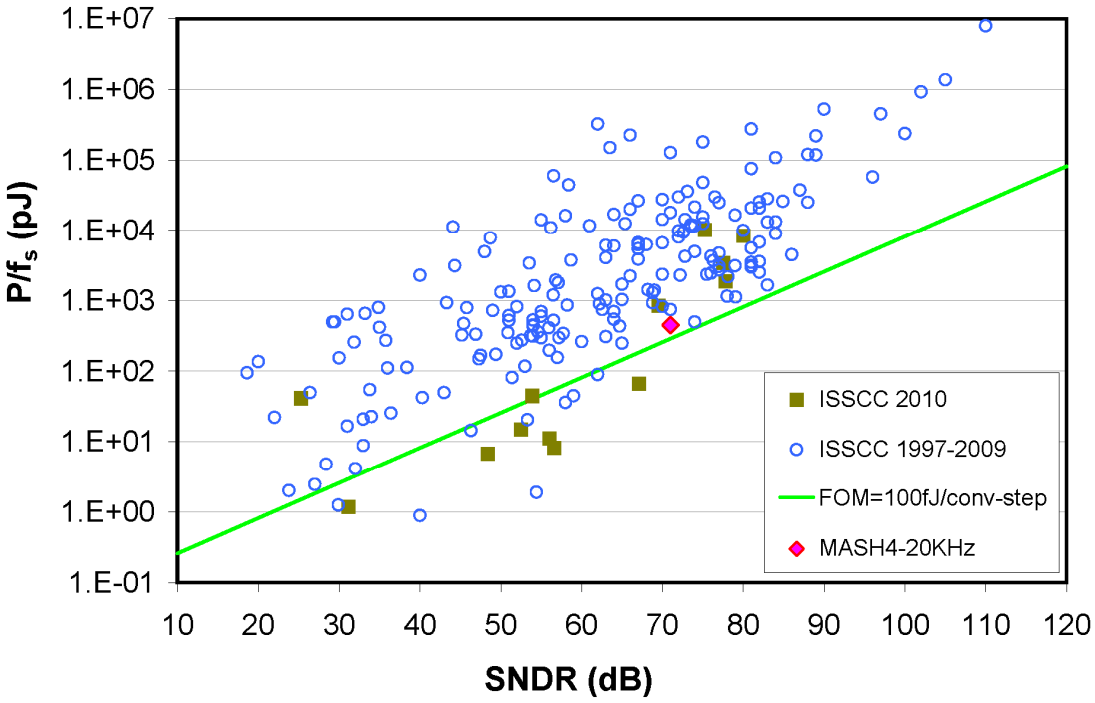


Fig. 7.16: State of the art in the ADC design

VI. CONCLUSION

A. Summary

This dissertation work made contributions in the following four aspects:

1. A suite of high performance self-biased inverter amplifiers: they can be utilized to replace the conventional Opamp in SC circuits for achieving high power and area efficiency.

2. The floating CDS technique: the floating CDS technique is tailored for improving the gain-linearity performance of the inverter amplifiers in the realization of SC circuits. For the delta-sigma ADC design, it is demonstrated that the floating CDS technique can improve the accuracy of the loop filters, lower the in-band noise floor, and suppress harmonic distortions.

3. The first inverter amplifier-based MASH architectures: two design topologies have been demonstrated. One is based on the high gain amplifier without CDS; the other is based on low gain amplifiers with CDS. This provides additional degree of freedom to choose for different requirements on power efficiency, silicon overhead, and design complexity.

4. A complete inverter amplifier-based SC circuit design methodology: the proposed inverter amplifier-based design methodology not only shows high power efficiency and design flexibility for delta-sigma modulators, but also demonstrates the potential for other low power and high speed SC circuits in further scaled CMOS processes.

B. Future Work

The following list enumerates some important steps that will be done in the future to further improve the ADC performance and gain deeper understanding of the delta-sigma modulation.

1. Investigate other system architectures of the delta-sigma ADC, such as feedforward structure, continuous time filter, or multi-bit quantizer.
2. Optimize the new inverter amplifier and the two-stage version in MASH architecture with CDS for achieving better performance.
3. Implement the decimation filter in Verilog and combine with the analog part.
4. Quantitatively analyze the variance tolerance of the inverter amplifiers. This part is important for explicitly understanding their operation principles.
5. Incorporate the amplifier nonlinear characteristics into the system modeling. Also, the nonlinear gain effect on the in-band noise floor may be revealed.
6. More thorough system modeling in Matlab. Most of the innovations and contributions come from the system level, not the circuit level.
7. Review the fundamental control theory and digital signal processing. Delta-sigma is only one of their applications.
8. Study nonlinear feedback system theory. Right now there are no analytical solutions for most of the delta-sigma modulators, and simulation is still the primary tool.

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Appendix

Matlab codes for characterizing the 2nd order modulator

```
function spectrum1(tmp, OSR, fbin, fs)

% spectrum(v, N, OSR, fbin)
% written by Le Wang
tmp=tmp';
v=reshape(tmp,32*1025,1);
v=v*2-1;
N=32000;
w=hann(N);
w1=norm(w,1);
V=fft(w.*v(1:32000))/(w1/2);

nb=3;
signal_bins=fbin+[-(nb-1)/2:(nb-1)/2];
inband_bins=0:N/2/OSR;
noise_bins_sndr=setdiff(inband_bins,[signal_bins 0 1]);
noise_bins_snr=setdiff(inband_bins,[signal_bins 0 1 [3*fbin-
1:3*fbin+1]]);
sndr=dbp(sum(abs(V(signal_bins+1)).^2)/sum(abs(V(noise_bins_sndr+
1)).^2))
snr=dbp(sum(abs(V(signal_bins+1)).^2)/sum(abs(V(noise_bins_snr+1)
).^2))

figure(1); clf;
semilogx([1:N/2]/N*fs,dbv(V(2:N/2+1)),'b','Linewidth',1);
grid on;
```

Matlab codes for characterizing the 4th order MASH prototypes

```
function spectrum(tmp, OSR, fbin, fs)

% spectrum(v, N, OSR, fbin)
% written by Le Wang, May 2010
tmp=tmp';
v=reshape(tmp,32*2050,1);
v1=v(1:32800);
v2=v(32801:65600);
v1=v1*2-1;
v2=v2*2-1;
vm=2*v1(3:32002)-2*v1(2:32001)+v1(1:32000)+6*(v2(3:32002)-
2*v2(4:32003)+v2(5:32004));
N=32000;
w=hann(N);
w1=norm(w,1);
V1=fft(w.*v1(1:32000))/(w1/2);
V2=fft(w.*vm)/(w1/2);

nb=3;
signal_bins=fbin+[-(nb-1)/2:(nb-1)/2];
inband_bins=0:N/2/OSR;
noise_bins_sndr=setdiff(inband_bins,[signal_bins 0 1]);
noise_bins_snr=setdiff(inband_bins,[signal_bins 0 1 [2*fbin-
1:2*fbin+1] [3*fbin-1:3*fbin+1]]);
sndr1=dbp(sum(abs(V1(signal_bins+1)).^2)/sum(abs(V1(noise_bins_sn
dr+1)).^2))
snr1=dbp(sum(abs(V1(signal_bins+1)).^2)/sum(abs(V1(noise_bins_snr
+1)).^2))
sndr2=dbp(sum(abs(V2(signal_bins+1)).^2)/sum(abs(V2(noise_bins_sn
dr+1)).^2))
snr2=dbp(sum(abs(V2(signal_bins+1)).^2)/sum(abs(V2(noise_bins_snr
+1)).^2))


figure(1); clf;
semilogx([1:N/2]/N*fs,dbv(V1(2:N/2+1)),'b','Linewidth',1);
hold on;
semilogx([1:N/2]/N*fs,dbv(V2(2:N/2+1)),'r','Linewidth',1);
grid on;
```