# A MULTI-DIMENSIONAL ANALOG GAUSSIAN RADIAL BASIS CIRCUIT

**Luke Theogarajan and L. A. Akers**
Center for Solid State Electronics Research
Arizona State University
Tempe, AZ
85287-5706

e-mail: lakers@asu.edu

## ABSTRACT

**Gaussian basis function(GBF) networks are powerful systems for learning and approximating complex input-output mappings. Networks composed of these localized receptive field units trained with efficient learning algorithms have been simulated solving a variety of interesting problems. For real-time and portable applications however, direct hardware implementation is needed. We describe simulated and experimental results from the most compact, low voltage analog Gaussian basis circuit yet reported. We also extend our circuit to handle large fan-in with minimal additional hardware. We show a SPICE simulation of our circuit implementing a multivalued exponential associative memory (MERAM).**

## 1. INTRODUCTION

Neurons with response characteristics that are locally tuned to a particular range of the input variable have been found in many parts of the central nervous system[1]. Examples include cells in the somatosensory cortex that respond selectively to stimulation from localized regions of the body surface, and orientation selective cells in the visual cortex that respond selectively to stimulation which are both local in retinal position and local in angle of object orientation[2].

Computer simulations of GBF networks are sufficient for many applications. However, hardware implementation of these systems are mandatory for many real-time, or low power, portable applications such as vision and speech recognition, robotics, and numerous other interactive control and signal processing applications. For these reason, we have developed a compact, low voltage, analog circuit implementation of the GBF network.

This paper first reviews the existing circuits that implement Gaussian basis functions. Then, we discuss our circuit including experimental data from a fabricated chip. To illustrate the usefulness of the approach, we describe an application using GBFs. Lastly, we summary our contribution.

## 2. EXISTING GAUSSIAN BASIS CIRCUITS

In the past few years there have been a number hardware implementations of the radial basis function in analog[3-6], and pulse forms[7].

The design by Delbruck [6] is shown in Fig. 1. It has been used in visual processing, and as a similarity computing element. It is based on a simple current correlator as shown in Fig. 2 which implements the function:

$$I_{out} = S\frac{I_1 I_2}{I_1 + I_2} \tag{1}$$

where:

$$S = \frac{(W/L)_{middle}}{(W/L)_{outer}} \tag{2}$$

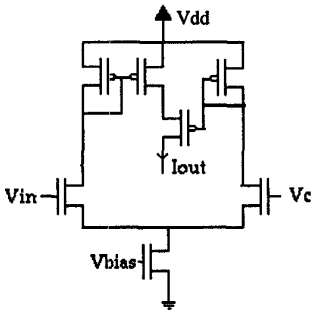


Fig. 1: The bump circuit of Delbruck.

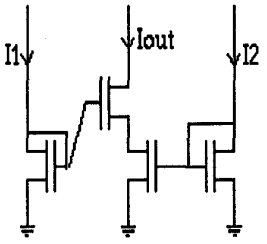


Fig. 2: The simple current correlator.

If the input currents to the current correlator are the limb currents of a differential amplifier given by:

0-7803-3073-0/96/$5.00 ©1996 IEEE

$$I_1 = I_b \frac{1}{1+e^{-\kappa\Delta V}}$$
$$I_2 = I_b \frac{1}{1+e^{\kappa\Delta V}} \quad (3)$$

where $\Delta V = V_1 - V_2$, then substituting this in the current correlator relationship provides:

$$I_{out} = I_b \frac{S}{4} \sec h^2\left(\frac{\kappa\Delta V}{2}\right) \quad (4)$$

This function gives a bell shaped curve which resembles a Gaussian.

Anderson et al.[5] have designed the analog VLSI radial basis circuit shown in Fig. 3. They have used the property that the current through the CMOS inverter resembles a Gaussian of the input voltage with the center occurring at Vdd/2. Our design philosophy is similar to theirs, but with some fundamental differences that will be discussed later.

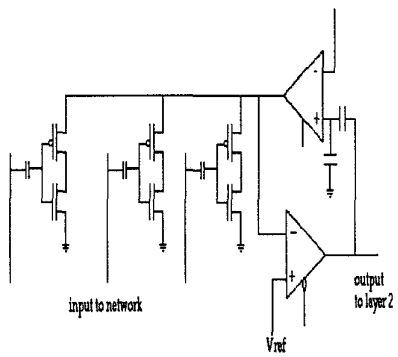


Fig. 3: The circuit used by Anderson et al.

## 3. THE MULTI-DIMENSIONAL GAUSSIAN BASIS CIRCUIT

When two transistors are connected in series, there occurs a self correlation of currents as discussed above, and if the currents have a differential or complementary nature a bump output results[6]. One way of implementing this differential or complementary nature is to use a differential amplifier. An alternate method is to use a device which has a complementary characteristic to the same input voltage. PMOS and NMOS devices have such complementary characteristics. By using this inherently complementary nature we have been able to design a circuit which approximates a Gaussian surface. The circuit is shown in Fig. 4. The input to the circuit is Vin-Vc, where Vc is the center. We plan to store this center using the floating gate transistor synapse as presented in Ref. [8]. In order to use the exponential relationship between the input voltage and output current, we operate our circuit mostly in the subthreshold region of operation. One way to achieve this is to lower the supply voltage such that both devices operate in the subthreshold region. However, this results in a very small current for all the input voltage swing. We have developed a method for the circuit to be in the subthreshold voltage region of operation for the tails of the output current, and be in the saturated above threshold voltage region for the peak of the output current. This gives an excellent peak-to-valley ratio, and good current drive. We do this with a non-linear resistor, in our case by a drain connected PMOS transistor. The PMOS load also facilitates the mirroring of the current to the output transistor.

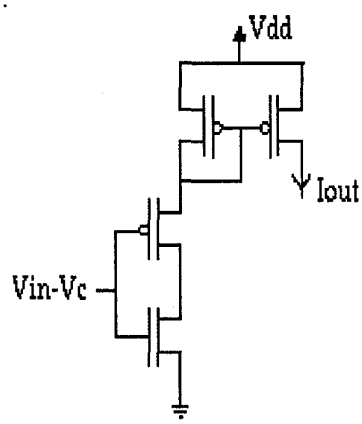


Fig. 4: Gaussian basis circuit

The extension of our circuit to the multi-dimensional case relies on the property of multiplication of Gaussians gives a Gaussian. By multi-dimensional we mean having multi-inputs with one overall output. The circuit is shown in Fig. 5.

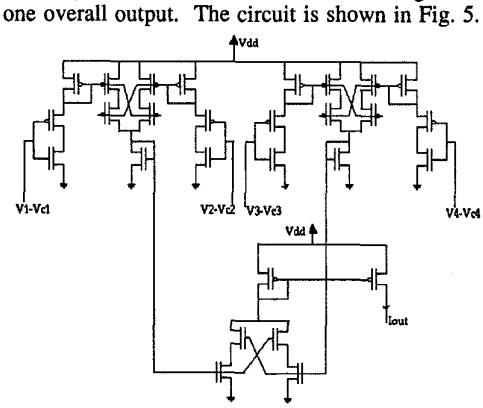


Fig. 5: The Multi-dimensional Gaussian circuit. The circuit is shown for 4 inputs. The same principle can be used to extend this to n inputs.

## 4. EXPERIMENTAL RESULTS

The chips were fabricated in the MOSIS 2-$\mu$m Nwell process. One chip had many one input Gaussian circuits with various transistor sizing, and another chip had 12 input circuits. The input to chip was a sawtooth from 0-3V. We made all measurements with Vc equal to 0V. The results from our chip for the one dimensional case for various sizings is shown in Fig. 6.

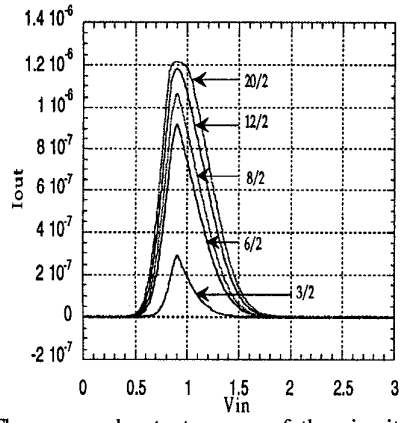


Fig. 6: The measured output curves of the circuit for equal PMOS and NMOS transistor sizing of 20/2, 3/2 for the largest to the smallest current peaks. The input to the circuit was with Vc equal to zero. This was done to observe the built-in center.

The 12 input multi-dimensional Gaussian circuit was tested as follows. Eleven inputs were tied together and the twelfth input was manually stepped through a voltage range from 0 to 2V in steps of .1V using a resistor string. These results are shown in Fig. 7.

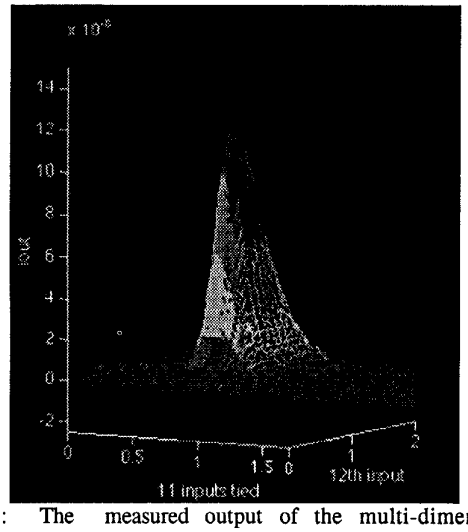


Fig. 7: The measured output of the multi-dimensional Gaussian circuit. 11 inputs are tied together. The 11 inputs are fed a sawtooth and the 12th input is manually stepped using a resistor string.

## 5. APPLICATION

The Gaussian basis circuit can be used in Gaussian radial basis classifiers. We show a SPICE simulation of a circuit implementing a multivalued exponential recurrent associative memory(MERAM)[12]. A MERAM is a high capacity associative memory.

This application employs a multi-dimensional Gaussian basis circuit as a similarity computing element. Our implementation is a variation of the implementation presented in [10]. The only modification is we have replaced their similarity computing element with our circuit. The block diagram of the circuit used is shown in Fig. 8. The exponentation and the weighted average are obtained by using a follower aggregator[11].

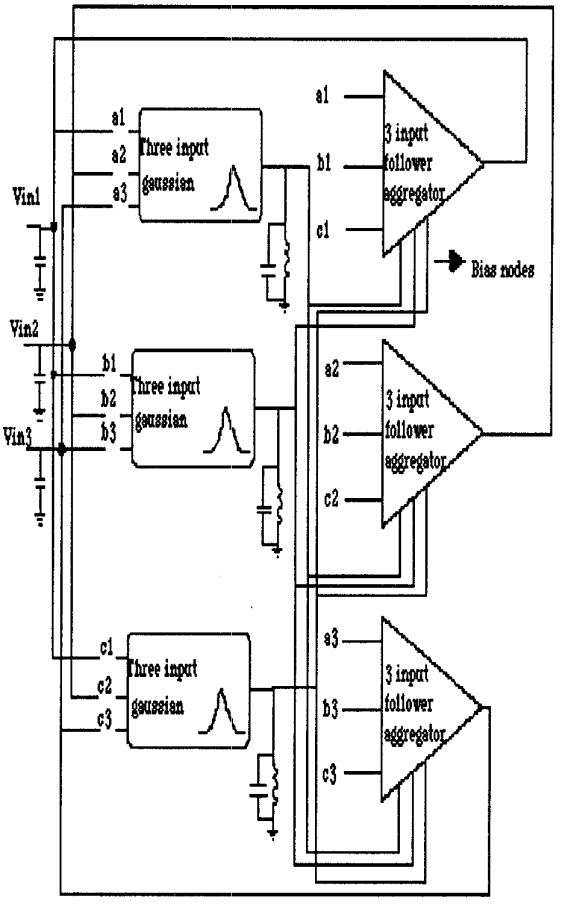


Fig. 8: Block diagram of MERAM circuit

A three input, three output, MERAM was simulated. Three patterns of three components were stored. For the first simulation, case 1, the stored patterns were

$$\begin{pmatrix} 1 & 1 & 1 \\ 1.5 & 1.5 & 1.5 \\ 2 & 2 & 2 \end{pmatrix}$$

The pattern applied to the input of the network was $(1.5 \quad 1.7 \quad 1.2)$. The network settled into the stored pattern $(1.5 \quad 1.5 \quad 1.5)$. This is shown in Fig. 9.

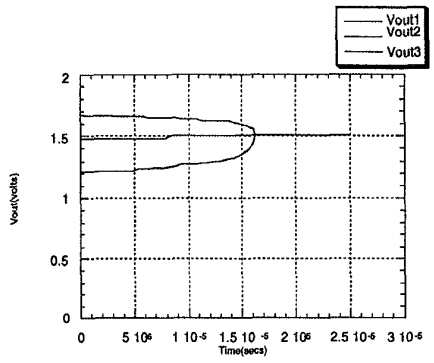


Fig. 9: The output of the MERAM network as a function of time for case 1.

## 6. CONCLUSION

Gaussian basis functions are universal approximators. We have built, fabricated and tested a very compact electronic implementation of such a function. We have also implemented a multidimensional extension of our circuit. We have shown simulations of a recurrent neural network, which behaves as an associative memory, using our multidimensional circuit.

## 7. REFERENCES


1. J. Moody, and C. Darken, "Fast Learning in Networks of Locally-tuned Processing Units", Neural Computation 1, 1989, 281-294.
2. J. Moody, and C. Darken, "Learning with Localized Receptive Fields", Proceeding of the 1988 Connectionist Models Summer School, D. Touretzky, G. Hinton, and T. Sejnowski, eds., Morgan-Kaufmann Publishers, San Mateo, CA.
3. T. Delbruck, "Bump Circuits", Caltech *Internal Document,* CNS Memo 26,1993.
4. Joongho Choi, Bing J. Sheu, and Josephine C.-F. Chang, " A Gaussian Synapse Circuit for Analog VLSI Neural Networks", *IEEE Trans. on VLSI Systems*, Vol.2, March 1994, pp. 129-133.
5. J. Anderson, J. C. Platt, and D. B. Kirk, " An Analog VLSI Chip for Radial Basis Functions", In S. J. Hanson, J. D. Cowan, and C. L. Giles,*Advances in Neural Information Processing Systems,*, Vol. 5, San Maetro, CA; Morgan Kaufmann Publishers Inc., 1993, pp. 765-772.
6. S. S. Watkins and P. M. Chau, "A Radial Basis Function Neurocomputer Implemented with Analog VLSI Circuits", *Proc. IEEE/INNS Int. Joint Conf. Neural Net.*, vol. II, pp. 607-612, Baltimore, MD, 1992.
7. S. Churcher, A. F. Murray and H. M. Reekie, "Programmable Analogue VLSI for Radial Basis Function Networks", *Electronics Letters*, 2nd September 1993, Vol. 29, No. 18. pp. 1603-1605.
8. P. Hasler, C. Diorio, B. Minch, C. Mead, " Single Transistor Learning Synapse with Long Term Storage", *Proc. IEEE International Symposium on Circuits and Systems*, vol. 3, pp., Seattle, Washington, 1995.
9. T. D. Chieuh and H. K. Tsai, "Multivalued Associative Memories Based on Recurrent Networks", *IEEE Trans. on Neural Networks*, vol4, no. 2, pp. 364-366, Mar 1993.
10. R-J. Huang and T. D. Chieuh, "Circuit Implementation of the Multivalued Exponential Recurrent Associative Memory", *World Congress on Neural Networks*, vol II, 1994, pp. 618-623.
11. C. Mead, *Analog VLSI and Neural Systems*, Addison-Wesley, Reading MA,1989.